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1 Introduction

The ADA-08 IP module of ACTIS Computer S.A. represents a highly integration on a single size IP, with support for a wide range of digital and analog I/O, divided in three sections :

- o A counter/timer and parallel I/O unit (CIO). This section provides two general-purpose 8-bit ports, one special-purpose 4-bit ports, and three 16-bit counter/timers.

- o An octal 12-bit digital to analog converter (DAC). This function provides eight single-ended buffered analog outputs in bipolar modes, which will directly accept, to drive an analog load on the DAC outputs.

- o A 12-bit+sign analog to digital converter (ADC). This function provides eight single-ended or four differential analog inputs for unipolar signals. An on-chip 8-word RAM can store the conversion sequence for up to eight acquisitions through the on-chip eight-input multiplexer.

The ADA-08 is compatible with the VITA-4 IP module specification.

2 Summary of features

- Single-size IP module.
- Compatible with the VITA-4 IP Module specification.

- Two general-purpose 8-bit ports.
- One special-purpose 4-bit ports.
- Three 16-bit counter/timers.
- Flexible pattern-recognition logic for interrupt generation.
- All signals in TTL levels.

- Octal 12-bit digital to analog conversion.
- Integral non linearity of ±2 LSB.
- Settling time less than 35 µs.
- On-board output amplifiers.
- Output voltage range: ±10 V

- Octal 12-bit + sign analog to digital converter.
- Up to 140 kSample/s throughput.
- On-chip multiplexer and instruction sequencer.
- Conversion accuracy of ±1 LSB.
- Settling time less than 5 µs.
- Single-ended and differential input modes.
- Input voltage range : ±10V (standard version)
  Factory option : ±5 V, 0 to +10 V and 0 to +5 V (min quantity required)
- Monitoring functions.
- Auto calibration and diagnostic mode.
- On-chip 32-word FIFO.
- External trigger capability.

- On-board two +5 V precision voltage reference.
- Industrial temperature range option (-40 to +85 °C).

3 Description

The CIO section of ADA-08 contains two general-purpose 8-bit ports, one special-purpose 4-bit and three 16-bit counter/timers.
All I/O signals, TTL levels, are directly connected from CIO controllers to the IP 50-pin I/O connector.

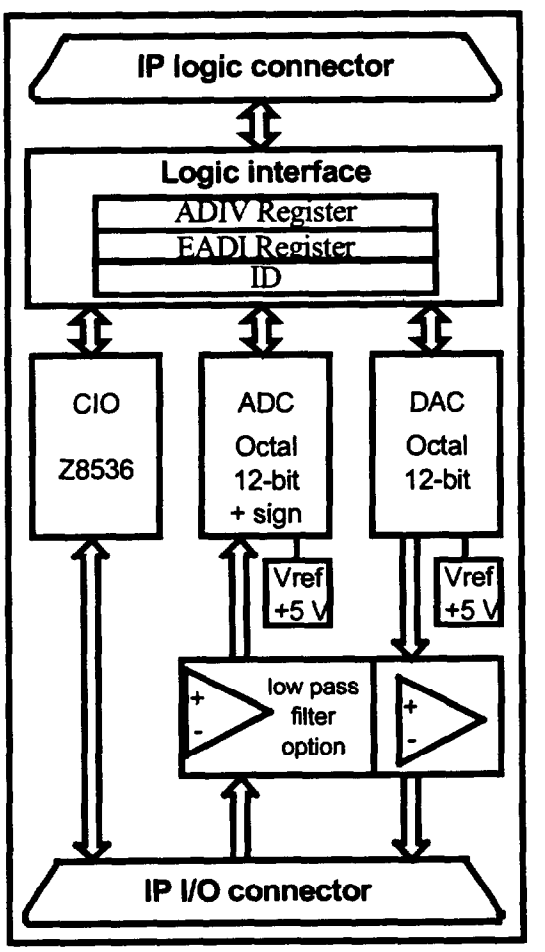
The DAC function is designed on the MP7613 (12-bit) digital to analog converter. Each DAC output is followed by an analog amplifier, to directly drive an analog load. Each output voltage range is ±10 V.
The modules includes a precision voltage reference reference (25 ppm/°C maximum temperature drift), factory calibrated, for digital to analog conversion and analog acqisition.

The ADC function is based on the LM12H458 analog to digital converter from National Semiconductor. This device offers very useful capabilities for acquisition operations: monitoring functions, on-chip FIFO, auto-calibration and diagnostic mode, programmable acquisition time and conversion rates. This device also provides a sequencer, which executes up to eight instructions. Each instruction defines the internal multiplexer selection, the conversion resolution, the acquisition time and the timer capability.
The ADC function provides a voltage range for each analog input between ±10 V (standard version).
(Factory option for min qty: ±5 V, 0 to +10 V and 0 to +5 V).
The LM12H458 also provides single-ended and differential input modes.

3.1 Block diagram

The hardware architecture of the ADA-08 is divided in six general main sections:

- The IP bus interface, controlling the timing access of the peripheral controllers.
- The CIO controller, Zilog Z8536.
- The MP7613 digital to analog converter.
- The LM12H458 analog to digital converter.
- The analog output amplifiers.
- The analog input amplifiers and optionally low pass filter.



3.2 IP spaces

The following table gives the four ADA-08 memory spaces.

IP space	Devices
MEMORY	No access
IDENTIFICATION	IP identification codes
I/O	• CIO registers • DAC Data registers • DAC Control register • ADC Data registers • ADC control register • ADC Interrupt vector register • ADC Enable interrupt vector register
INTERRUPT ACK.	CIO Interrupt acknowledge cycle ADC Interrupt acknowledge cycle

The base address of these spaces depends on the IP carrier.

3.2.1 I/O space

The CIO controller is mapped into the IP I/O space. Data and command registers of the CIO controller are placed on 4 consecutive addresses (8-bit data path).

I/O space adr.	Register	Description
CIO controller		
$51	PCDR	Port C Data Register
$53	PBDR	Port B Data Register
$55	PADR	Port A Data Register
$57	CR0	Control Register 0

All port configurations are defined with the CIO control registers. The data registers allow the value of each ports to be accessed directly.

The DAC converter is mapped into the IP I/O space and provides eight 16-bit data registers and one 8-bit command registers.

I/O space adr.	Access	Bus wide	Register	Description
$40	R/W	16-bit	DAC0	DAC code for channel 0
$42	R/W	16-bit	DAC1	DAC code for channel 1
$44	R/W	16-bit	DAC2	DAC code for channel 2
$46	R/W	16-bit	DAC3	DAC code for channel 3
$48	R/W	16-bit	DAC4	DAC code for channel 4
$4A	R/W	16-bit	DAC5	DAC code for channel 5
$4C	R/W	16-bit	DAC6	DAC code for channel 6
$4E	R/W	16-bit	DAC7	DAC code for channel 7
$79	W	8-bit	DACREG	DAC Output Update and reset register

The LM12458 interrupt vector registers are mapped into the IP I/O space.

I/O space adr.	Access	Bus wide	Register	Description
LM12H458 registers				
$00	R/W	16-bit	RAM0	Instruction RAM0
$04	R/W	16-bit	RAM1	Instruction RAM1
$08	R/W	16-bit	RAM2	Instruction RAM2
$0C	R/W	16-bit	RAM3	Instruction RAM3
$10	R/W	16-bit	RAM4	Instruction RAM4
$14	R/W	16-bit	RAM5	Instruction RAM5
$18	R/W	16-bit	RAM6	Instruction RAM6
$1C	R/W	16-bit	RAM7	Instruction RAM7
$20	R/W	16-bit	CONF	Configuration register
$24	R/W	16-bit	ENINT	Enable Interrupt register
$28	R	16-bit	INTST	Interrupt Status register
$2C	R/W	16-bit	TIMER	Timer register
$30	R	16-bit	FIFO	Conversion FIFO
$34	R	16-bit	LIMIT	Limit status register
$61	R/W	8-bit	ADIV	ADC Interrupt vector register
$71	R/W	8-bit	EADI	Enable ADC Interrupt register

3.2.2 ID space

The identification space is defined as follows:

ID space adr.	Description	value
$01	Ascii "I"	$49
$03	Ascii "P"	$50
$05	Ascii "A"	$41
$07	Ascii "C"	$43
$09	Manufacturer identification	$99
$0B	Module type	$24
$0D	Revision module	*
$0F	Reserved	$00

* See below for description.

The four first bytes contain the ASCII text "IPAC". This clearly identifies the ROM beginning.
The manufacturer code $99 identifies ACTIS IP.
The ADA-08 device is defined by the module type byte $24.
The next byte identifies the IP revision, in accordance with the following definition.

Revision	ASCII car.	hex. value
First	"_" (space)	$5F
Next	"A", "B", ...	$41, $42, ...

The byte $0F is reserved for future extension.

3.2.3 Wait state cycles

The following tables gives the number of wait states asserted in each IP space.

Space	Wait state	
	Read	Write
Identification	0	N.A.
I/O CIO		
o CIO registers	4	4
o Interrupt acknowledge	5	N.A.
I/O ADC		
o ADC registers	2	2
o Interrupt Vector (IV) register	0	0
o Enable interrupt Vector (EIV) register	0	0
o Interrupt acknowledge	0	N.A.
I/O DAC		
o DAC data registers	6	2
o DACOU register	N.A.	2
o DACRST register	N.A.	0

4 Characteristics

4.1 CIO

Symbol	Parameters	Test conditions	Min	Max	Unit
V_{IH}	Input high voltage		2	Vcc + 0.3	V
V_{IL}	Input low voltage		-0.3	0.8	V
V_{OH}	Output high voltage	I_{OH}=-250 µA	2.4		V
V_{OL}	Output low voltage	I_{OL}=+2 mA I_{OL}=+3.2 mA		0.4 0.5	V
I_{CC}	Vcc supply current			310	mA
PCLK	Peripheral clock			4	MHz

4.2 DAC

Symbol	Parameters	Test conditions	Min	Max	Unit
N	Resolution			12	bit
INL	Integral non linearity	Ta=25 °C		±2	LSB
DNL	Differential non linearity	Ta=25 °C		±1	LSB
ZOFS	Bipolar zero offset	Ta=25 °C		±2	LSB
_E	Channel-to-channel max. error (all code)	Ta=25 °C		±1	LSB
ME	All channels maximum error	Ta=25 °C		±4	LSB
MES	All channel error span	Ta=25 °C		5	LSB
τ_{sd}	Settling time from DAC output writing to DAC output valid	Zero to Full scale. (20 V step)		55 (typ. 35)	µs

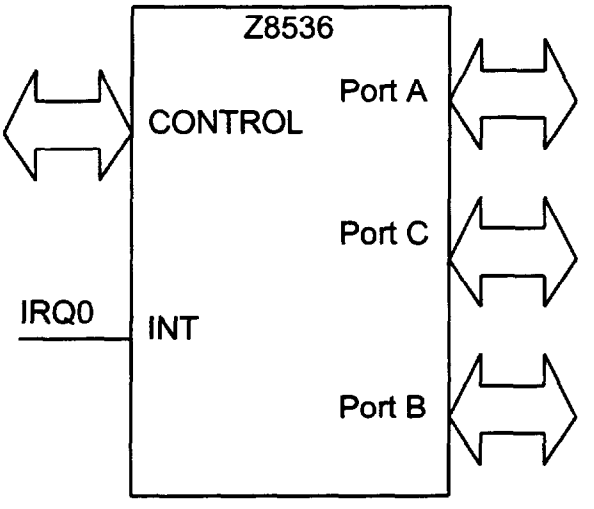
Symbol	Parameters	Test conditions	Min	Max	Unit
R_{LOAD}	Analog load	±10 V range ±5 V range 0 to +10V range	2 400 2		kΩ Ω kΩ
TCVo	Voltage reference temperature coefficient			25	ppm/°C
Vref	Voltage reference	FS DAC0 min. error		typ. 5	V
Vcc	Vcc analog voltage		11.4	12.75	V
Vee	Vee analog voltage		-12.75	-11.4	V
Vdd	Vdd digital voltage		4.5	5.5	
Icc	Positive supply current		90	210	mA
Iee	Negative supply current		90	210	mA
Idd	Digital supply current		95	120	mA

4.3 ADC

Symbol	Parameters	Test conditions	Min	Max	Unit
N	Resolution	After auto-cal.		12+sign	bit
INL	Integral non linearity	After auto-cal.		±1.5	LSB
DNL	Differential non linearity	After auto-cal.		±1	LSB
ZOFS	Bipolar zero offset	After auto-cal.		±1.5	LSB
FSE	Full-scale error	After auto-cal.		±2	LSB
Tc	Conversion time	12-bit + sign 9-bit + sign		11 5.3	µs
Tc	Conversion time	12-bit + sign 8-bit + sign		11 5.3	µs
Tacq	Acquisition time	12-bit + sign 8-bit + sign		2.3 0.6	µs
Tz	Auto-zero time	Sequencer S2		19	µs
Tcal	Full calibration time	Sequencer S2		1.2	ms
	Throughput rate	Standard version.		140	kS/s
τ_{sd}	Settling time, analog interface propagation delay.	10 V step		2	µs
Z_{IN}	Impedance input on input multiplexer		10		kΩ
Rs	Source resistance to LM12458 converter			< 10	Ω
TCVo	Voltage ref. temp. coefficient			25	ppm/°C
CLK	LM12458 clock	Standard version		typ . 8	MHz
Vref	Voltage reference			typ. 5	V
Vcc	Vcc analog voltage		11.4	12.75	V
Vee	Vee analog voltage		-11.4	-12.75	V
Vdd	Vdd digital voltage		4.5	5.5	V
Icc	Positive quiescent current			50	mA
Iee	Negative quiescent current			40	mA
Idd	Digital quiescent current			180	mA
Ta	Operating ambient temperature	Standard version	0	+70	°C
Tstg	Storage temperature		-60	+150	°C

5 Zilog CIO Z8536

The ADA-08 IP contains a Z8536 devices, and the following description gives you the features of these CIO controller.
The Z8536 device provides two general-purpose 8-bit ports (port A and B), one special-purpose 4-bit port (port C), and three 16-bit counter/timers (timer 1 to 3).



The CIO controller provide an interrupt IRQ0 connected to *IntReq0* of the IP logic interface.

5.1 General-purpose ports

These ports can be programmed either as a handshake-driven, and as single or as double buffered port (input, output, or bi-directional) with the direction of each bit individually programmable. These two ports (ports A and B) can also be linked to form a 16-bit I/O port with handshake. Each port can generate an interrupt when a specific pattern-recognition is detected. This pattern offers a very large flexibility for a specific OR/AND condition, the polarity and the transition detection (state or edge) are independently programmable for each bit-port.
The second port (port B) allows an external access to the first and second software counter/timers (counter/timers 1and 2).
To program these capabilities, both ports contain 12 registers. The command and status registers define the primary port functionality. Two registers are used to define the port specification and handshake modes. The I/O data is accessed through the input, output and buffer registers. The data direction, data path polarity and special I/O control registers allow programming each bit. The pattern-recognition is defined with the pattern polarity, pattern transition and pattern mask registers.

5.2 Special-purpose port

The function of this port (port C) is defined in accordance with the role of the general-purpose ports. This port can provide either handshake lines for the general-purpose ports, either an external access to the third counter/timer (counter/timers 3) or either conventional I/O lines.
Only three registers (data path polarity, data direction, and special I/O control) are necessary to control the port C when the general-purpose ports functionality (ports A and B) have been specified.

5.3 Counter/Timers

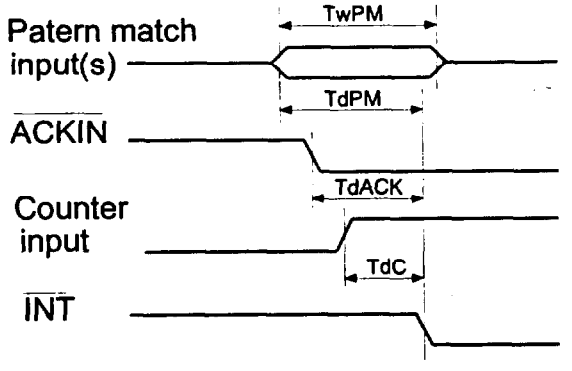
All the three counter/timers (counter/timers 1 to 3) are functionality identical.
Three output modes are available: pulse, one-shoot, and square-wave. The operating mode of the counter/timer can be programmed either as retriggerable or as non-retriggerable.
Up to four control lines are provided for timer/counter operation : counter input, gate input, trigger input, and counter/timer output.
Each counter/timer provides a time-constant register containing the initial value of the down-counter. At any time the current count register shows the content of the down-counter. Two other registers are used the control register to set the timer/counter configuration, and the timer/counter status register.

5.4 CIO Interrupt function

Five registers control the CIO interrupt functions: the master interrupt control, three interrupt vector registers, and the current interrupt vector register.

5.5 Interrupt timing

The following timing descriptions give the delay for interrupt generation.
In bit port mode, an interrupt is generated when the pattern-recognition is detected.
In handshake port operation, the external ACKIN signal strobes the input data into the CIO and an interrupt is activated to indicate to the host that a valid input data is present.



Symbol	Parameters	Min	Max	Unit
TwPM	Pattern match input valid (bit port)	750		ns
TdPM	Pattern match to INT delay (bit port)		1.3	µs
TdACK	ACKIN to INT delay (port with handshake)		3.1	µs
Td	Counter input to INT delay (timer mode)		1.2	µs