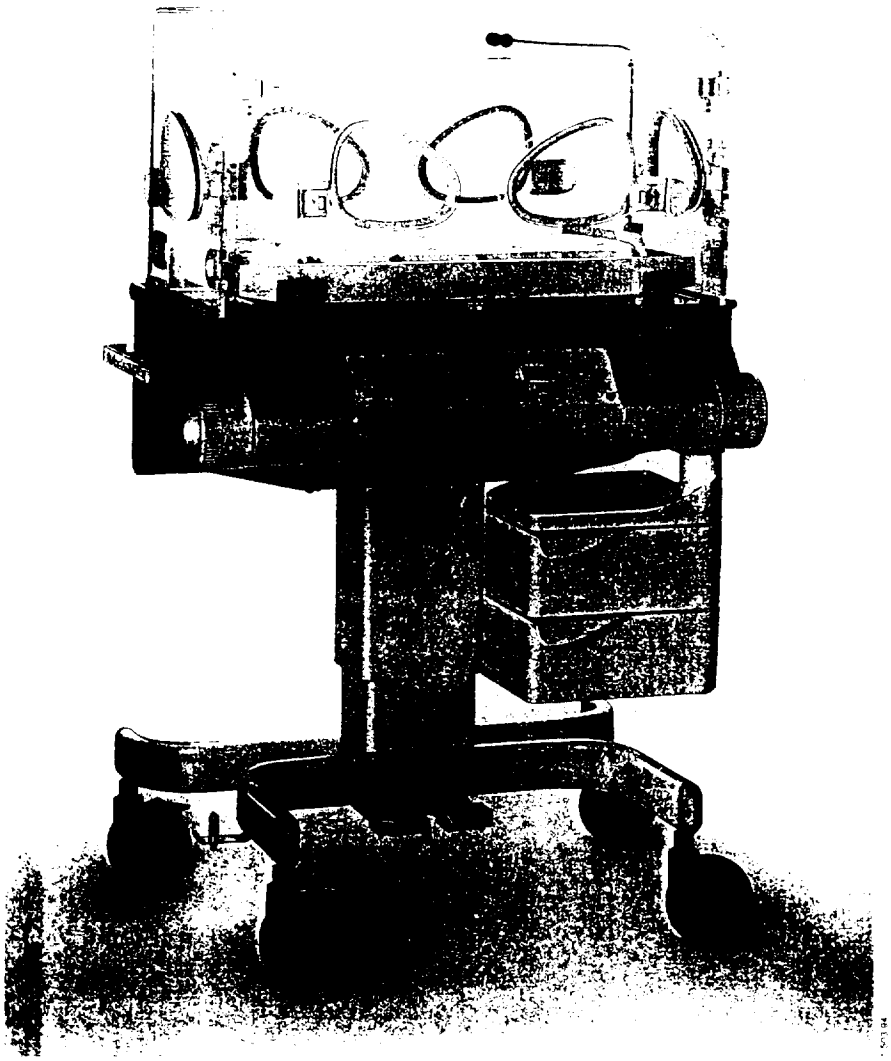
INCUBATEUR NÉONATAL



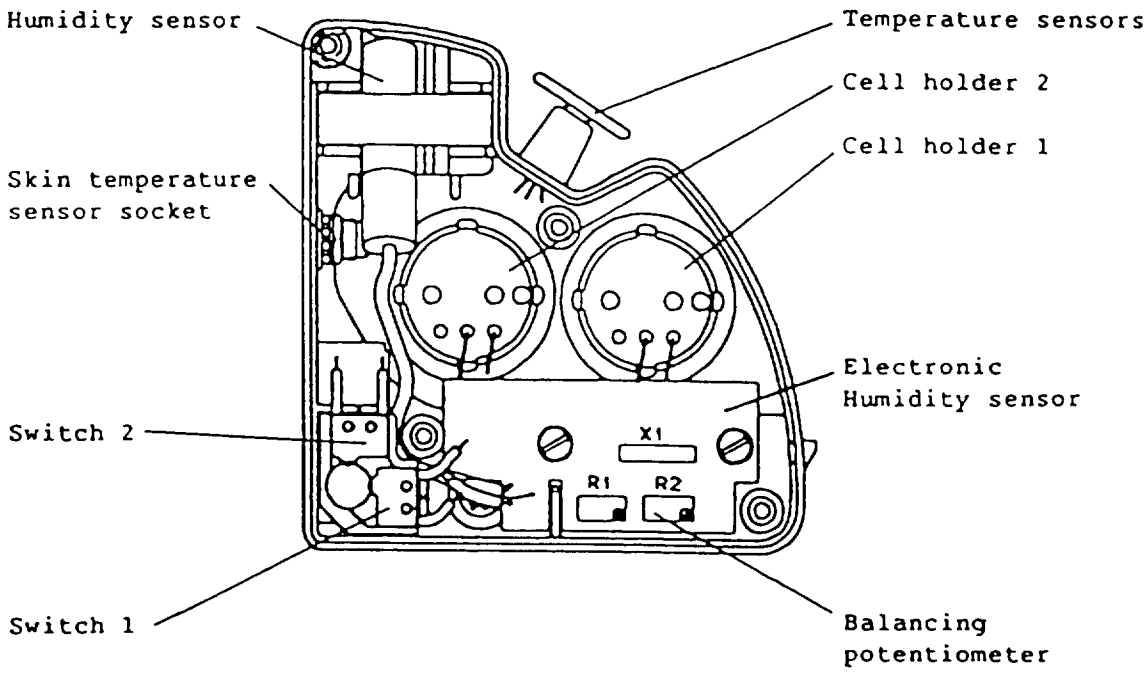
Code examen 51025504	B.E.P ELECTRONIQUE	Dossier ressources
	E.P.3 TRAVAUX DE SYNTHESE	SESSION 2000

3.4 Environmental sensor housing (only Inc. 8000 IC)

3.4.1 Intended use

The Incubator sensor serves measurement of the climatic conditions inside Incubator 8000. The air temperature, O_2-concentration and the relative air humidity are monitored. A skin temperature sensor may be connected to devices which are equipped accordingly.

3.4.2 Arrangement



3.4.3 Humidity sensor

In the environmental sensor housing a capacitive humidity sensor with the evaluation electronics is installed. The output voltage is:

$$U_{humidity} = \frac{7.1}{100\ \%} \times \text{rel. H. (\%)} + 1.05\ V$$

3.4.4 Microswitch

The position of the environmental sensor housing is evaluated via two microswitches in four positions:

1 sensor housing swivelled in

2 sensor housing partly swivelled in

3 sensor housing hinged

4 sensor housing removed from the hinge

3.5 Skin temperature sensor

The skin temperature sensor is a NTC.

In addition to the recognition "sensor plugged in" a short-circuiting link is installed in the plug.

T (°C)	R (Ohm)
33.0	1588.3
36.0	1411.3
38.0	1293.3

3.4.3 Detailed description

3.4.3.1 Temperature sensors

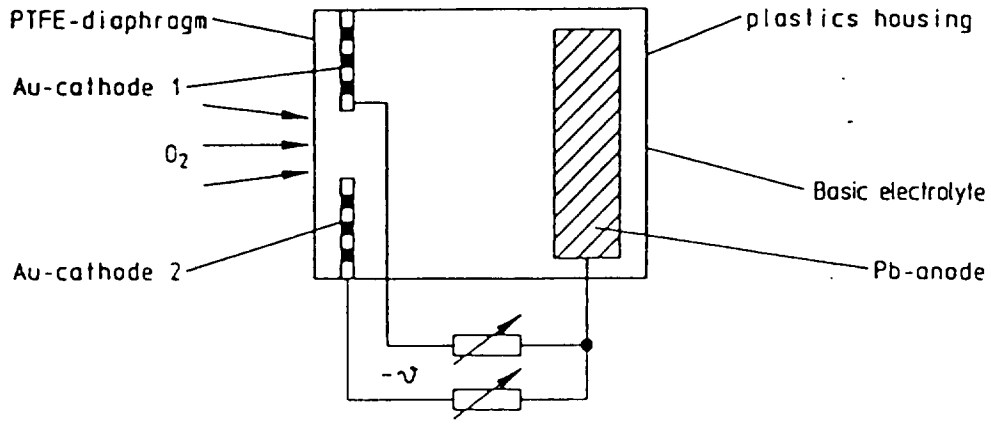
Both temperature sensors are NTCs.

t (°C)	R (Ω)		t (°C)	R (Ω)
10	9950,00		25	5000,00
11	9485,30		26	4786,10
12	9044,20		27	4582,50
13	8626,30		28	4388,80
14	8230,20		29	4204,40
15	7854,70		30	4028,70
16	7498,50		31	3861,20
17	7160,50		32	3701,60
18	6839,70		33	3549,60
19	6535,20		34	3404,60
20	6246,00		35	3266,30
21	5970,80		36	3134,40
22	5709,40		37	3008,60
23	5460,90		38	2888,50
24	5224,70		39	2773,90

DrägerService
Medizintechnik
Medical Systems

The sensor is designed according to the fuel cell principle as double cell, i.e. it is an electrochemical cell which builds up a voltage due to an ionic current.

The cell comprises the capsule with the electrolytes, the lead anode and the gold cathode with teflon foil.



Thermistors

The oxygen to be measured diffuses through the teflon diaphragm, reacts at the gold cathodes and produces lead oxide and H_2O at the lead anode. During this chemical process an electric voltage is produced which is proportional to the oxygen partial pressure. The gold cathode is polarized positive, while the lead anode is negative. Since the lead anode is converted it has a limited lifetime. The internal resistance is determined by the electrode surface, the oxygen diffusion rate and the distances. It is also dependent on the sensor lifetime. In normal condition it is 700 Ohm. Like most of the chemical processes this one is also dependent on the temperature. Because of this temperature-independent resistors are connected in parallel to the sensor which correct the measuring-circuit voltage in conjunction with the internal resistance.

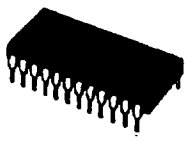
SGS-THOMSON MICROELECTRONICS

HCC/HCF4067B
HCC/HCF4097B

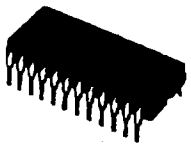
ANALOG MULTIPLEXER/DEMULTIPLEXER

4067B–SINGLE 16-CHANNEL
4097B–DIFFERENTIAL 8-CHANNEL

- LOW ON RESISTANCE 125Ω (typ.) OVER 15 Vp-p SIGNAL INPUT RANGE FOR V_{DD} - V_{SS} = 15V
- HIGH OFF RESISTANCE: CHANNEL LEAKAGE OF ±10pA (typ.) @ V_{DD} - V_{SS} = 10V
- MATCHED SWITCH CHARACTERISTICS: ΔR_{ON} = 5Ω (typ.) FOR V_{DD} - V_{SS} = 15V
- VERY LOW QUIESCENT POWER DISSIPATION UNDER A DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS: 0.2μW (typ.) @ V_{DD} -V_{SS} = 10V
- BINARY ADDRESS DECODING ON CHIP
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIE CMOS DEVICES"



EY
(Plastic Package)



F
(Ceramic Package)

M1
(Micro Package)

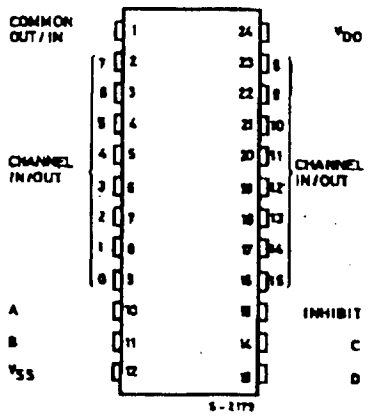
C1
(Chip Carrier)

ORDER CODES :

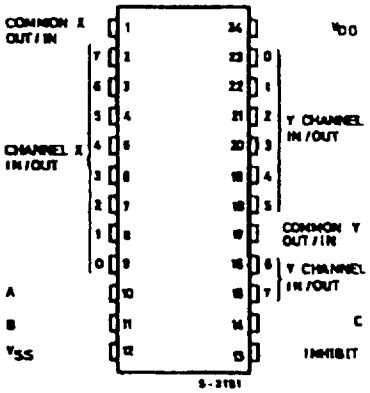
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

PIN CONNECTIONS

4067B



4097B



TRUTH TABLES FOR HCC/HCF4067B

A	B	C	D	INH	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

TRUTH TABLE FOR HCC/HCF4097B

A	B	C	INH	SELECTED CHANNEL
X	X	X	1	None
0	0	0	0	0X 0Y
1	0	0	0	1X 1Y
0	1	0	0	2X 2Y
1	1	0	0	3X 3Y
0	0	1	0	4X 4Y
1	0	1	0	5X 5Y
0	1	1	0	6X 6Y
1	1	1	0	7X 7Y

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD} *	Supply Voltage: HCC Types HCF Types	-0.5 to +20 -0.5 to +18	V V
V_I	Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for Top = Full Package Temperature Range	200 100	mW mW
T_{op}	Operating Temperature: HCC Types HCF Types	-55 to +125 -40 to +85	°C °C
T_{stg}	Storage Temperature	-65 to +150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage: HCC Types HCF Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature: HCC Types HCF Types	-55 to +125 -40 to +85	°C °C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditios V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	Value T_{LOW} * Min.	T_{LOW} * Max.	25 °C Min.	25 °C Typ.	25 °C Max.	T_{HIGH} * Min.	T_{HIGH} * Max.	Unit
I_L	Quiescent Supply Current	HCC types				5		5		0.04	5		150	µA
						10		10		0.04	10		300	
						15		20		0.04	20		600	
						20		100		0.08	100		3000	
		HCF types				5		20		0.04	20		150	
						10		40		0.04	40		300	
						15		80		0.04	80		600	
SWITCH														
R_{ON}	On Resistance	HCC types	$0 \le V_I \le V_{DD}$	0	0	5		800		470	1050		1300	Ω
						10		310		180	400		580	
						15		200		125	240		320	
		HCF types	$0 \le V_I \le V_{DD}$	0	0	5		850		470	1050		1200	
						10		330		180	400		520	
						15		210		125	240		300	
ΔON	Resistance ΔR_{ON} (Between any two channels)			0	0	5				10				Ω
						10				10				
						15				5				
OFF (•) Channel Leakage Current	Any Channel OFF	HCC types		0	0	18		100		±0.1	100		1000	µA
	All Channel OFF (common OUT/IN)	HCC types		0	0	18		100		±0.1	100		1000	
	Any Channel OFF	HCF types		0	0	15		300		±0.1	300		1000	
	All Channel OFF (common OUT/IN)	HCF types		0	0	15		300		±0.1	300		1000	
C	Capacitance Input Output for 4067 Output for 4097 Feedthrough				-5	5				5 55 35 0.2				pF
CONTROL														
V_{IL}	Input Low Voltage		= V_{DD} thru 1KΩ	V_{EE}=V_{SS} R_L =1KΩ to V_{SS} I_{IS} < 2µA (on all OFF channels)		5		1.5			1.5		1.5	V
						10		3			3		3	
						15		4			4		4	
V_{IH}	Input High Voltage					5	3.5		3.5			3.5		V
						10	7		7			7		
						15	11		11			11		
I_{IH} I_{IL}	Input Leackage Current	HCC types	V_I = 0/18V			18		±0.1		$±10^{-3}$	±0.1		±1	µA
		HCF types	V_I = 0/15V			15		±0.3		$±10^{-3}$	±0.3		±1	
C_I	Input Capacitance		Any Address or Inhibit Input							5	7.5			pF

• Determined by minimum feasible leakage measurement for automatic testing

* T_{LOW} = -55 °C for HCC device: -40 °C for HCF device.

* T_{HIGH} = +125 °C for HCC device: +85 °C for HCF device.

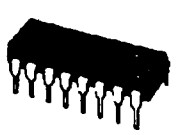
The Noise Margin for both "1" and "0" level is: 1 V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, 2.5 V min. with V_{DD} = 15 V

SGS-THOMSON MICROELECTRONICS

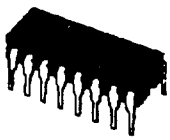
M54HCT138
M74HCT138

3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED
  t_{PD} = 16 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS138



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

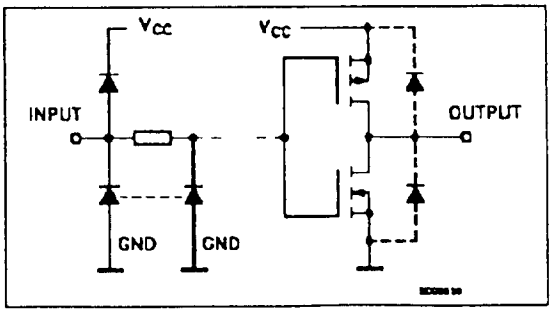
ORDER CODES :

M54HCT138F1R	M74HCT138M1R
M74HCT138B1R	M74HCT138C1R

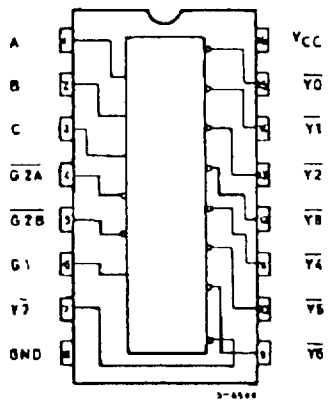
DESCRIPTION

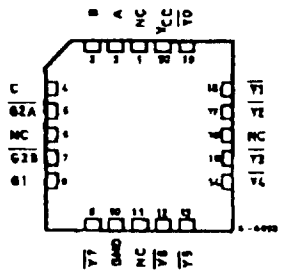
The M54/74HC138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low. If enable input G1 is held low or either $\overline{G2A}$ or $\overline{G2B}$ is held high, the decoding function is inhibited and all the 8 outputs go high. Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems. All inputs are equipped with protection circuits against static discharge and tran- sient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

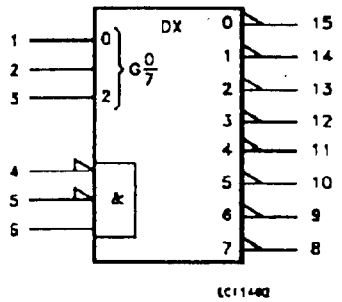
INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X : Don't Care

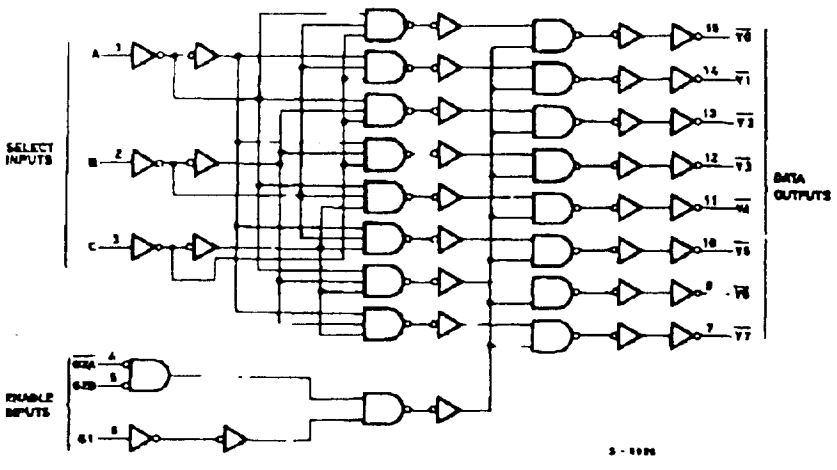
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$, $\overline{G2B}$	Enable Inputs
6	G1	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM

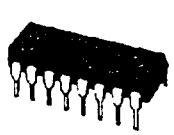


SGS-THOMSON MICROELECTRONICS

M54HCT139
M74HCT139

DUAL 2 TO 4 DECODER/DEMULTIPLEXER

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS139



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

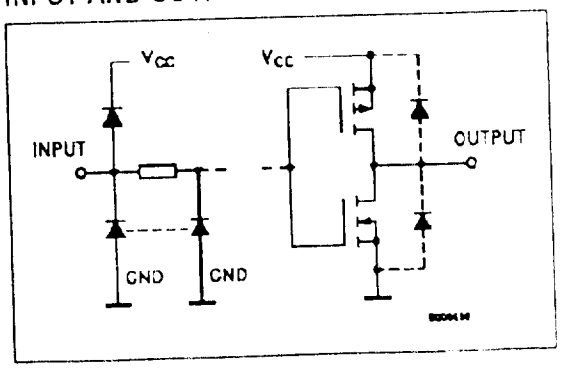
ORDER CODES :

M54HCT139F1R M74HCT139M1R
M74HCT139B1R M74HCT139C1R

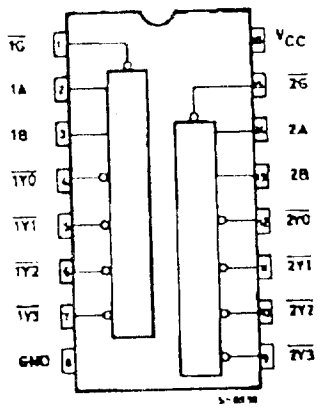
DESCRIPTION

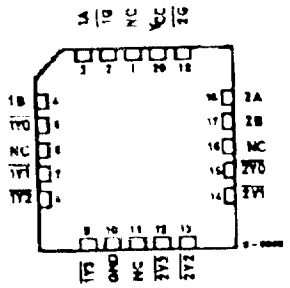
The M54/74HCT139 is a high speed CMOS DUAL TWO LINE TO FOUR LINE DECODER/DEMULTIPLEXER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The active low enable input can be used for gating or as a data input for demultiplexing applications. While the enable input is held high, all four outputs are high independently of the other inputs. All inputs are equipped with protection circuits against static discharge and transient excess volt-age. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^{2}MOS systems with TTL and NMOS components. They are also plug in replacements for

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



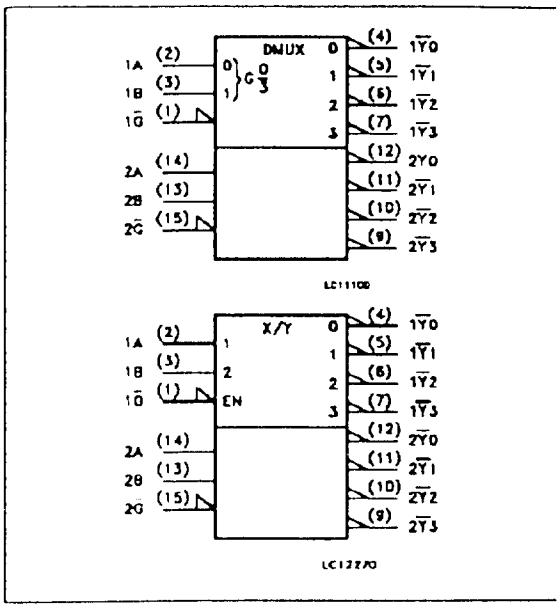


NC =
No Internal
Connection

TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
$\overline{G}$	B	A	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	$\overline{Y}_0$
L	L	H	H	L	H	H	$\overline{Y}_1$
L	H	L	H	H	L	H	$\overline{Y}_2$
L	H	H	H	H	H	L	$\overline{Y}_3$

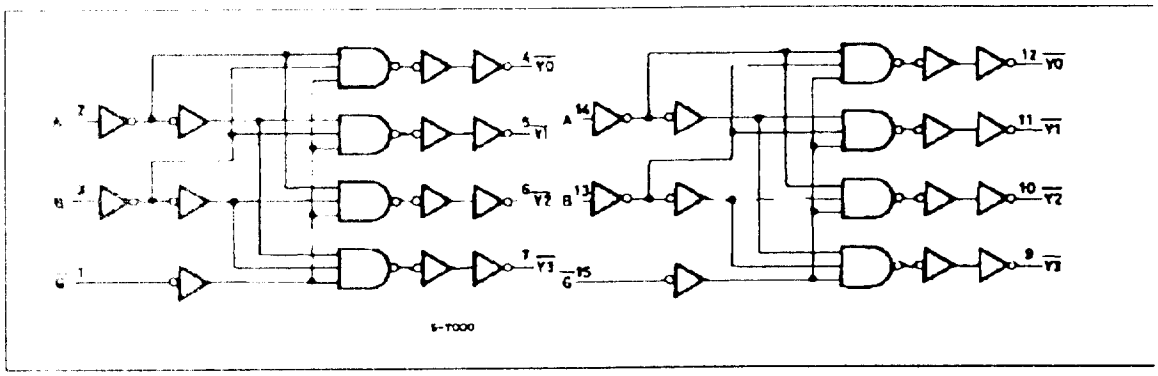
IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{G}$, $2\overline{G}$	Enable Inputs
2, 3	1A, 1B	Address Inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	Outputs
14, 13	2A, 2B	Address Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW = 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

PIA 6821 : Description des registres internes.

INTERNAL CONTROLS

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA 2	Control Register Bit CRB 2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Details of possible configurations of the Data Direction and Control Register are as follows.

DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. A Data Direction Register bit set at "0" configures the corresponding peripheral data line as an input; a "1" results in an output.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the [illegible] Table 2.

TABLE 2 – CONTROL WORD FORMAT

	7	6	5	4	3	2	1	0
CRA	IRQ[illegible]	[illegible]	[illegible]		[illegible] Control	Data [illegible] A[illegible]	CA[illegible]	Control
CRB	IRQB[illegible]	[illegible]	[illegible]		[illegible]	DDRB A[illegible]	[illegible]	Control

Data Direction Access Control Bit (CRA-2 and CRB-2) – Bit 2 in each Control Register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

[illegible] of [illegible] CRA-7, CRB-6, and CRB-7 – [illegible] interrupt flag bits are set by active transitions of [illegible] on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits [illegible] from the MPU Data Bus and are [illegible] Read Peripheral Data Operation on [illegible].

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

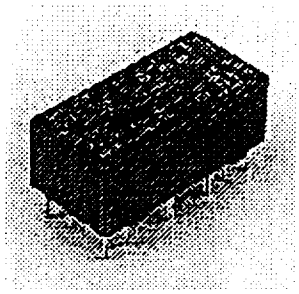
CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

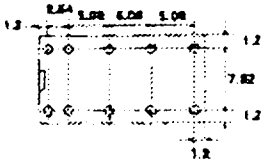
Notes
1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-0 (CRB-0) is written to a "one".

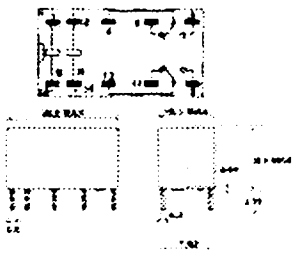
MOTOROLA Semiconductor Products Inc.

Relais bistables - type G6AK

Omron







- Modèles bistables, polarisés, à 2 bobines.
- Haute sensibilité, commande possible en circuits numériques.
- Dimensions très réduites.
- Importante rigidité diélectrique (conforme à FCC §68) pour utilisation dans les équipements de télécommunications.
- Possibilité de montage côte à côte.
- Prévus pour le nettoyage aux ultrasons, et faible f.e.m.

Spécifications techniques

Bobine - puissance consommée env. 200 mW (sauf 24 V: 180 mW)

Contact

- charge nom. 125 V c.a./0,3 A, 30 V c.c./1 A (résistive)
- courant de passage 2 A
- courant max. 3 A
- tension de fonctionnement 250 V c.a., 220 V c.c.
- pouvoir de coupure:

125 VA/60 W (charge résistive)

62,5 VA/30 W (charge inductive)

- charge min. 10 m V c.c./0,01 mA

Résistance de contact 50 mΩ max.

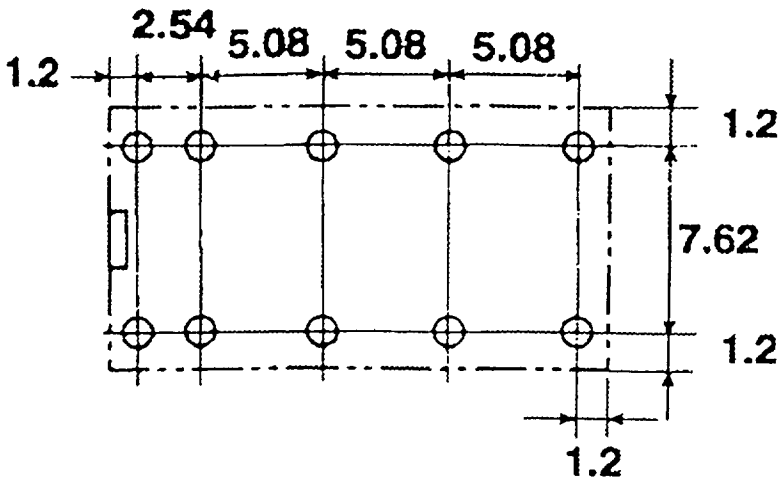
Durée de vie mécanique 100 x 10^6 manoeuvres min.

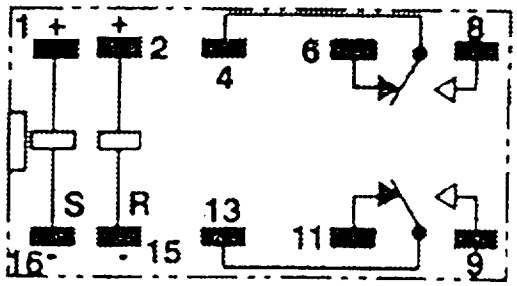
Format DIL 16 broches

Dimensions (mm):
20,2 max. x 10,1 max. x h 8,4 (y compris pieds de lavage 0,64 mm)

Température d'utilisation -40°C à +70°C

Homologations UL et CSA





réf. Omron	code commande	tension bobine	I nom. (mA)	résistance bobine (Ω)
G6AK-234P-ST-5DC	**369-595**	5 V c.c.	36	139
G6AK-234P-ST-12DC	**369-602**	12 V c.c.	15	800
G6AK-234P-ST-24DC	**369-618**	24 V c.c.	7,5	3200