

BTS INFORMATIQUE INDUSTRIELLE

Session 2001

Epreuve Etude d'un Système Informatisé

Système d'acquisition de température de bobinages

ANNEXES DU SUJET

Ces annexes sont communes à la première et à la deuxième partie du sujet.

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ANNEXE S1

Carte CPU BAB40 (extraits)

BAB-40/60

1 Specification

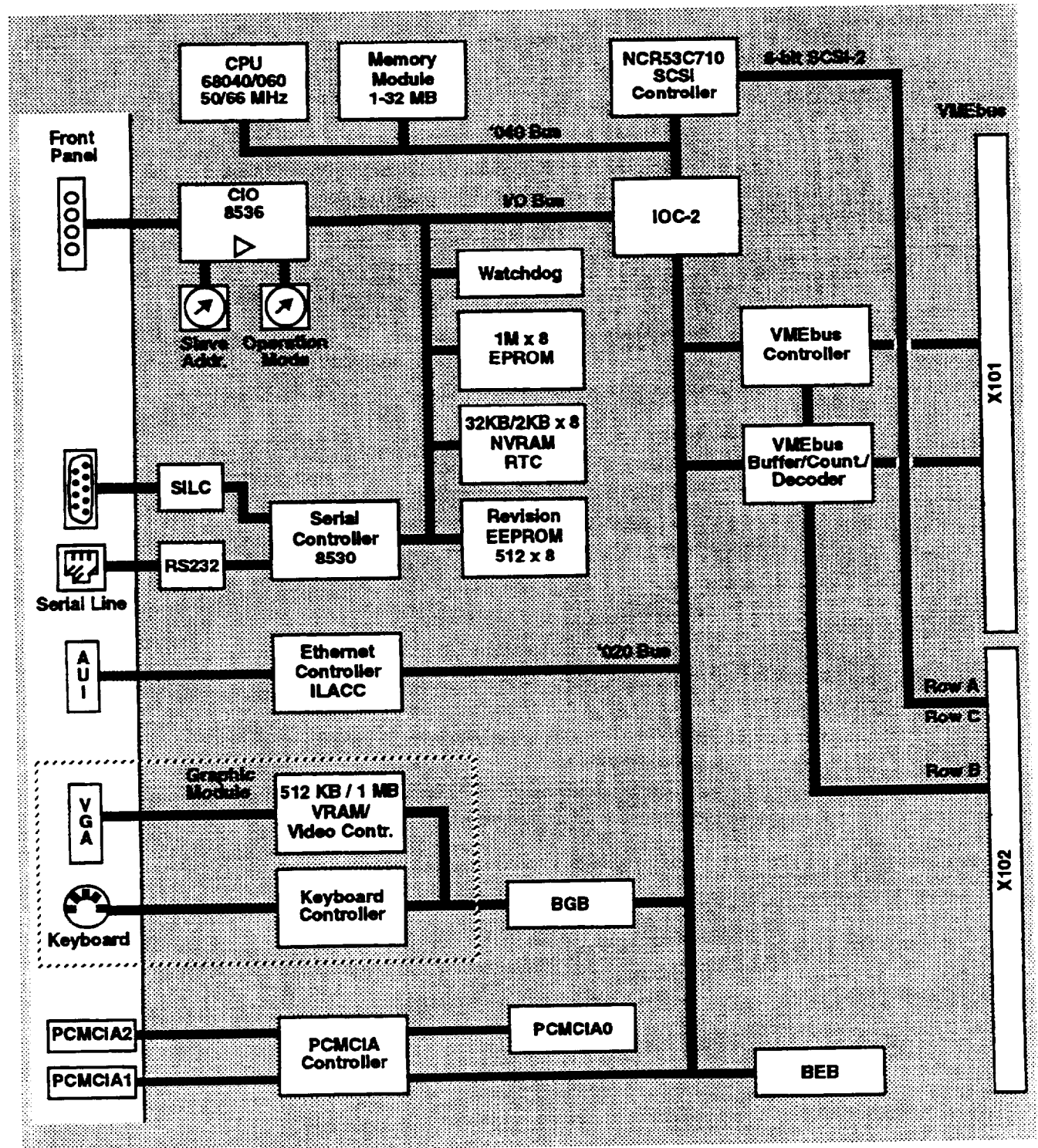
1 Specification

1.1 Main Features

- One 68(EC)040/060 CPU at 50 MHz or 66 MHz
- Memory
 - PS/2 SIMM memory module (1, 2, 8, 16, 32 MB) for data/program storage (44 MB/s at 33 MHz bus speed)
 - 2 KB SRAM and RTC for storage of variable system parameters MK48T12 (MK48T18/8 KB, DS1644/32 KB)
 - Up to 1 MB x 8 K EPROM
- Two PCMCIA sockets on front panel for two type I or II PC Cards or one type III PC Card (Flash, SRAM and ATA-HD only)
- One internal PCMCIA socket (type I, type II, or with some restrictions type III (Flash, SRAM and ATA-HD only))
- Ethernet interface (32-bit ILACC)
- VMEbus Interface Controller:
 - System controller and arbiter
 - VMEbus interrupter and interrupt handler
 - 32-bit slave BLT 20 MB/s
 - Master / slave write posting
- IOC-2 gate array:
 - 68040 to 68020 bus converter
 - Dynamic bus sizing for VMEbus and BEB
 - Translation of BLT into bursts on '040 bus to allow snooping of BLT cycles
 - Separate arbitration on '040 and '020 bus
 - I/O bus interface
 - Support for VMEbus UATs to allow snooping
 - Interface for a single byte-wide EPROM
- Three 16-bit timer / counter
- Two serial ports (RS 232, RS 422, RS 485)
- Smart SCSI-2 (NCR 53C710) interface with burst capability (max. transfer capacity 10 MB/s) and single-ended 8-bit SCSI data bus
- Two rotary switches for selection of operation modes and base address
- Status display on front panel
- Watchdog timer 130 ms ... 17 min
- BEB for interfacing to various mezzanine busses
- BGB for graphic and keyboard module

1.2 General Description

Figure 1: Block Diagram



3 Programmers Reference

3.1 Address Map

The BAB-40/60 is designed to utilize the entire 4 GB address range of the 68040/060 chip. Using the address modifier of the VMEbus, the address range may be enlarged by subdivision into data and program areas and / or user and supervisor areas. The BAB-40/60 recognizes two address areas: the local address space and the global VMEbus address space.

Table 23: Address Assignment of BAB-40/60

Address Range	Device	VMEbus Address Modifier	Cache ¹⁾	Burst ²⁾	Access Width [b]
\$0000.0000 - \$01FF.FFFF	Local RAM	local	Y	Y	32
\$0200.0000 - \$03FF.FFFF	Local RAM (mirrored)	local	N	Y	32
\$0400.0000 - \$05FF.FFFF	Video RAM	local	Y	N	32
\$0600.0000 - \$07FF.FFFF	Video RAM (mirrored)	local	N	Y	32
\$0800.0000 - \$FBFF.FFFF	VMEbus Extended	A32	N ³⁾	N	32/16/8
\$FC00.0000 - \$FC3F.FFFF	PCMCIA1	local	N	N	16/8
\$FC40.0000 - \$FC7F.FFFF	PCMCIA2	local	N	N	16/8
\$FC80.0000 - \$FCBF.FFFF	PCMCIA0	local	N	N	16/8
\$FCC0.0000 - \$FCFF.FFFF	Reserved	-	-	-	-
\$FD00.0000 - \$FDFF.FFFF	BEB0	local	N	N	32/16/8
\$FE00.0000 - \$FE7F.FFFF	BEB1	local	N	N	32/16/8
\$FE80.0000 - \$FEBF.FFFF	EPROM	local	Y	N	8
\$FEC0.0000 - \$FECF.FFFF	Local I/O	local	N	N	32/16/8
\$FED0.0000 - \$FEFF.FFFF	Reserved	-	-	-	-
\$FF00.0000 - \$FFFE.FFFF	VMEbus Standard I/O	A24	N	N	32/16/8
\$FFF0.0000 - \$FFFF.FFFF	VMEbus Short I/O	A16	N	N	16/8

1. Y = /TCI driven high, N = /TCI driven low.
2. Y = /TBI driven high, N = /TBI driven low.
3. Caching may be enabled via system control register.

ANNEXE S2

Carte d'extension VMOD-IO (extraits)

1. General

The VMOD-IO is a VMEbus-compatible carrier board for up to four plug-in modules with MODULbus-Interface. Even if the mother board is equipped with four modules, only one slot in the VME-system is Needed.

With use of the VMOD-IO the system integrator is able to build up VME-systems with flexible configurations for needs in industrial environment.

1.1 Specifications

- VMEbus nonintelligent carrier board for MODULbus
- double euro-card with A24/D16 VMEbus slave interface
- 4 plug-in sockets for MODULbus I/O
- different vector from each MODULbus socket
- jumper selectable interrupt level
- 2KByte short-I/O or standard-address range
- needs only one VME-Slot
- front panel and P2 connection of I/O lines
- optional on-board DC/DC converter to supply analog modules

1.2 Functional overview

The VMOD-IO carrier board can be equipped with a maximum of 4 MODULbus I/O-modules.

Every MODULbus socket has a 512byte address space and can be selected as byte-device or as word-device.

For integration in complex VMEbus-systems the VMOD-IO can be used within the Short-I/O address space or within the Standard memory address space.

The plug-in modules are able to cause a modified vectored interrupt to the VMEbus via the carrier board with selectable level and configurable vector. The vector holds information about the causing module in its 4 LSB's.

2. Addressing

The VMOD-IO uses 2048 bytes within the 64Kbyte wide Short-I/O or in the 16Mbyte wide Standard address range of the VMEbus.

2.1 Board-address

The basic address of the board can be set by using 2 code-switches in the SHORT address range and with 4 code-switches in the STANDARD address range.

Switch S1 corresponds to the address line A11, switch S2 to address lines A12 - A15, switch S3 to address lines A16 - A19 and switch S4 accordingly to address lines A20 - A23.

The selection of the address range can be ensured by jumper J4. If the SHORT address range is chosen, the address on the code-switches S3, S4 and on the corresponding address lines is irrelevant.

2.1.1 Example of setting

Example 1:

To select address 68xxH in the SHORT address range the code-switch S2 has to be set to "6" and code-switch S1 has to be set to "8".

Example 2 :

To select address 2568xxH in the STANDARD address range switch S4 has to be set to "2", switch S3 to "5", switch S2 to "6" and switch S1 to "8".

2.2 Address-modifiers

The VMOD-IO decodes the address modifiers which are specified by the VMEbus. This means that during an access on the AM-lines there must be a code which describes what sort of an access it is, i.e. USERDATA, SYSTEM I/O etc.

The VMOD-IO accepts User- and system- Short accesses with AM-codes 29H and 2DH and User/System Standard accesses with AM-codes 39H and 3DH. The choice is made by jumper J8, J9 and J10. Jumper J8 corresponds with AM3, J9 with AM4 and J10 with AM5. AM0 is set "high" and AM1 is set "low".

For Short-accesses the jumpers have to be set as follows:

J4 set to position 2-3

J10	J9	J8
1	0	1

0 = jumper set

For Standard-accesses the jumpers have to be set as follows :

J4 set to position 1-2

J10	J9	J8
1	1	1

0 = jumper set

2.3 Address-ranges

The addresses of the MODULbus-sockets are :

MODULbus socket	address
socket 0	0H - 1FFH
socket 1	200H - 3FFH
socket 2	400H - 5FFH
socket 3	600H - 7FFH

MODULbus addresses

ANNEXE S3

DOCUMENTATION VMOD TTL/O

VMOD TTL/O
MODULbus digital
Input / Output Module

JANZ Computer AG

General

The VMOD-TTL/O is an opto-isolated digital input/output module for MODULbus carrier-boards and is ideally suited for industrial control purpose where parallel inputs are required.

Only proven and reliable components are used in order to ensure perfect operation in industrial environments. The high standard in quality and manufacturing ensure a highly reliable product.

Specifications

- 20 bit TTL-level, opto-coupled inputs/outputs
- Single 4bit and double 8bit I/O channels
- In / output configurable per channel
- Max. 48mA open collector outputs
- 3x16bit counter/timer internally or externally controlled
- Interrupt on change of input state or input pattern
- Physically dimensions 55mm x 110mm

Functional Overview

The VMOD-TTL/O is a single module with MODULbus interface able to use on carrier boards for specific host computer bus system (VMEbus, PC/AT...)

The module is fitted with the Counter/Timer-I/O device (CIO) Z8536 from ZILOG. Thereby the module provides 20 parallel in- or outputs. These are divided in two channels of 8bit each and one channel of 4bit. Each channel is opto-isolated from system potential and is optionally configurable as input or output.

All of the inputs/outputs are connected to a 25pin D-Sub connector on the front of the module. Further on the inputs/outputs of channel B and channel C are led to a 20-pin I/O connector on the module for back panel connection of the carrier-board.

On the VMOD-TTL/O a pattern recognition logic is able to generate interrupts on a bit pattern or a rising or falling edge at the inputs of channel A or B. The 8 inputs of each channel can be logically combined by "AND" or "OR" functions. Further on interrupts can be generated by "zero count" of the counter/timer.

Addressing

The VMOD-TTL/O transmits or receives data on the low-byte data bus of the MODULbus carrier-board. It can be plugged on every MODULbus socket.

The module address can be determined as follows:
Board address + MODULbus socket + Module register

The module registers have the following addresses:

Relative Address	Function	Status
0	Port C's data register CIO	rd/wr
1	Port B's data register CIO	rd/wr
2	Port A's data register CIO	rd/wr
3	Control register CIO	rd/wr

Input- Output Configuration

All of the 20 inputs/outputs of the VMOD-TTL/O have TTL-level. They are realized on the hardware side via three drivers and opto-couplers, so that in- or outputs are available in two 8bit channels and in

one 4bit channel. Each channel is configurable as input or output by the user.

A corresponding commitment for the input/output of data at a later date has be supported by software in the right way.

The inputs/outputs are fitted with drivers of the type 74LS645-1 and opto-couplers of the type TLP-521. the open collector outputs are fitted with 4K7 pull-up resistors on the module, so that the user must only connect the external supply Vext for the outputs (Vext = 5V) for TTL-level, Vext must not exceed 35V).

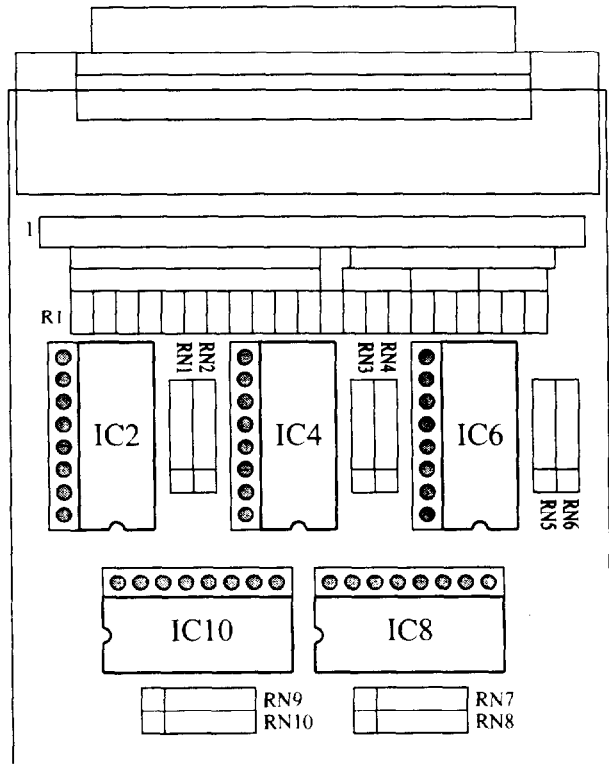
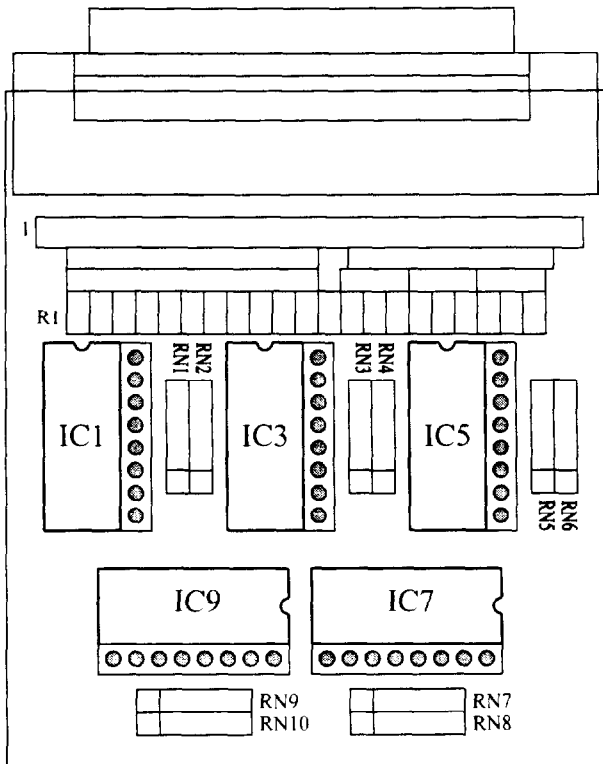
All inputs are related to a common external return potential GNDext. The input current is typically

8mA. In input mode the external supply Vext is not used.

The direction of the drivers i.e whether in- or output is decided by the jumpers J1 (port A), J2 (port B) and J3 (port C). The direction of the opto-couplers is decided by rotating the opto-coupler IC1 – IC4 (port A), IC5 – IC8 (port B) and IC9 – IC10 (port C).

For “receive”, which means that the I/O-channels have been programmed as input, the jumper J1 – J3 have to be open and the opto-couplers IC1, IC3, IC5, IC7 and IC9 have to be set as follows:

For “transmit”, which means that the I/O-channels have been programmed as output, the jumper J1 – J3 have to be set and the opto-couplers IC2, IC4, IC6, IC8 and IC10 have to be set as follows:



Each I/O channel is configurable as input or output independent of the other channels. The following table shows the jumper settings and opto-coupler placement for different I/O configurations:

Port A	Port B	Port C	J1	J2	J3	Opto-coupler placement
input	input	input	open	open	open	IC1, IC3, IC5, IC7, IC9
input	input	output	open	open	set	IC1, IC3, IC5, IC7, IC10
input	output	input	open	set	open	IC1, IC3, IC6, IC8, IC9
input	output	output	open	set	set	IC1, IC3, IC6, IC8, IC10
output	input	input	set	open	open	IC2, IC4, IC5, IC7, IC9
output	input	output	set	open	set	IC2, IC4, IC5, IC7, IC10
output	output	input	set	set	open	IC2, IC4, IC6, IC8, IC9
output	output	output	set	set	set	IC2, IC4, IC6, IC8, IC10

Pin-assignment

The 20 inputs/outputs are conducted to a 25 pins D-Sub connector on the module front. The pin assignment of the connector is show in the following table:

pin #	signal	pin #	signal
1	D0 (port A)	14	D3 (port C)
2	D2 (port A)	15	D1 (port C)
3	D4 (port A)	16	Vext (port B)
4	D6 (port A)	17	D7 (port B)
5	GNDext	18	D5 (port B)
6	D0 (port B)	19	D3 (port B)
7	D2 (port B)	20	D1 (port B)
8	D4 (port B)	21	Vext (port A)
9	D6 (port B)	22	D7 (port A)
10	GNDext	23	D5 (port A)
11	D0 (port C)	24	D3 (port A)
12	D2 (port C)	25	D1 (port A)
13	Vext (port C)		

More over the inputs are conducted via a 20 pins I/O connector to the back panel connector on the

MODULbus carrier-board. The pin assignment of the 20 pins I/O connector is as follows:

pin #	signal
1	Vext (port B)
2	Vext (port C)
3	D0 (port B)
4	D1 (port B)
5	D2 (port B)
6	D3 (port B)
7	D4 (port B)
8	D5 (port B)
9	D6 (port B)
10	D7 (port B)
11	D0 (port C)
12	D1 (port C)
13	D2 (port C)
14	D3 (port C)
15	GNDext
16	GNDext

Interrupt

The VMOD-TTL/O is fitted with a Z8536 (Counter Timer I/O) from Zilog. The CIO contains two independent 8bit wide bi-directional I/O ports and a 4bit wide special function I/O port (port C).

The inputs/outputs of the VMOD-TLL/O are realized by the 8bit port's A and B and by the 4bit port C of the Z8536.

All inputs of the port's A and B are able to generate interrupts to the MODULbus carrier-board via the interrupt line INT. With jumper INT the interrupts of the VMOD-TLL/O can be disabled (jumper open). The input bit's of port A and B can

be logically combined for the interrupt condition by a "AND" or "OR" function.

- The conditions for generating interrupts are:
- Input pattern
- Rising edge
- Falling edge
- Rising or falling edge
- "Zero count" of counter/timer

The interrupt vector must be configured on the MODULbus carrier-board, so that the interrupt vector register within the CIO device can not be used.

Technical Data

MODULbus connection
Digital inputs/outputs
Power supply
Power consumption
Operating temperature
Permissible humidity
Dimensions
Weight

Two 20pin connectors
Max. 20, opto-isolated
Vcc = 4.75V ... 5.25V
Typ. 0.25A
0 - 70°C
0% - 80%, non condens.
55mm x 112mm
ca. 100g

ANNEXE S4

Carte d'extension VMOD-GPIB (extraits)

1. Functional Overview

The JANZ General Purpose Interface Bus module VMOD-GPIB connects a VME- or IBM PC/XT/AT computer system to a general-purpose interface bus. The module is designed according to the industry standard ANSI/IEEE488.2.

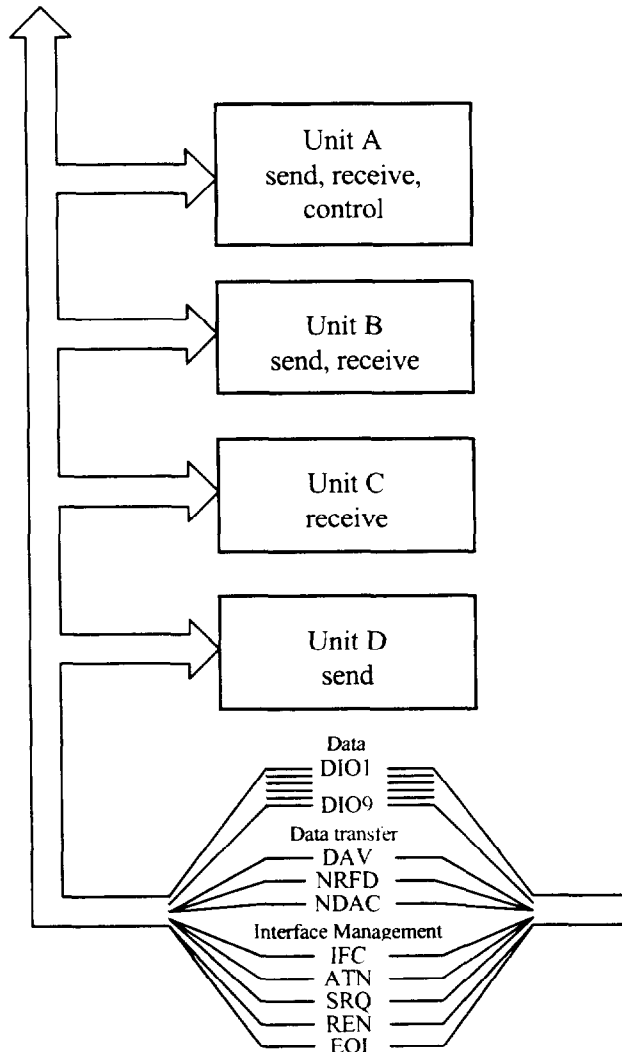


Figure 1-1: GPIB Bus Structure

The VMOD-GPIB converts every VME- or PC/AT computer system into an intelligent data acquisition or control unit. The parallel bus structure (8 data lines) guarantees high data throughput rates. The 3 wire handshake (DAV, NRFD, NDAC) eliminates any transfer errors. Another 5 wires (IFC, ATN, SRQ, REN, EOI) are for GPIB management purpose (see Figure 1-1).

Up to 15 GPIB-units are connectable on the same physical bus. A unit can be a 'Listener', a 'Talker' or a 'Controller'. The VMOD-GPIB has all 3 capabilities choosable by software.

- 1) receiving messages in the 'Listener'-mode
- 2) sending messages in the 'Talker'-mode
- 3) managing bus activities in the 'System Controller'-mode

2. Addressing

The VMOD-GPIB can be plugged in every MODULbus socket of the carrier board (MOD-AT, VMOD-IO, VMOD-IG, VMOD-40). The 16 internal registers (8 read / 8 write) of the GPIB-controller μ PD7210 are mapped in the module offset address range 00H-0EH. A write with any data to an offset address between 30H-3FH puts the VMOD-GPIB into the controller mode. In this mode, the module is able to drive the GPIB signals IFC (interface clear) and REN (remote enable). The controller mode is left by writing to an address between 20H-2FH. Each VMOD-GPIB register is byte or word addressable (see Table 2-1).

Register	Mode	Offset Address
Data In	read	00H
Data Out	write	00H
Interrupt Status 1	read	02H
Interrupt Mask 1	write	02H
Interrupt Status 2	read	04H
Interrupt Mask 2	write	04H
Serial Poll Status	read	06H
Serial Poll Mode	write	06H
Address Status	read	08H
Address Mode	write	08H
Command Pass Through	read	0AH
Auxiliary Mode	write	0AH
Address 0	read	0CH
Address 0/1	write	0CH
Address 1	read	0EH
End of String	write	0EH
...
Controller On	write	20H-2FH
Controller Off	write	30H-3FH

Table 2-1: VMOD-GPIB Register Addressing

3. Jumper Settings

The VMOD-GPIB module has only one jumper (J1), which enables the DMA feature when set. In this case, the MODULbus signals "DMRQ" (DMA Request) and "DMAK" (DMA AcKnowledge) take control over the data flow to or from the GPIB-Controller (refer to the NEC μ PD7210 description). Only the carrier board VMOD-IG supports DMA-transfer.

JUMPER J1	VMOD-GPIB Operating Mode
open	DMA disabled
closed	DMA enabled

Table 3-1: Jumper J1 Configuration