Inhibit Logic

The Inhibit Logic Section samples the OE and SEL signals on the falling edge of the clock and, in response to certain conditions (see Figure 10 below), inhibits the position data latch. The RST signal asynchronously clears the inhibit logic, enabling the latch. A simplified logic diagram of the inhibit circuitry is illustrated in Figure 11.

Bus Interface

The bus interface section consists of a 16 to 8 line multiplexer and an 8-bit, three-state output buffer. The multiplexer allows independent access to the low and high bytes of the position data latch. The SEL and $\overline{OE}$ signals determine which byte is output and whether or not the output bus is in the high-Z state. In the case of the HCTL-2000 the data latch is only 12 bits wide and the upper four bits of the high byte are internally set to zero.

Quadrature Decoder Output (HCTL-2020 Only)

The quadrature decoder output section consists of count and up/down outputs derived from the 4X decode logic of the HCTL-2020. When the decoder has detected a count, a pulse, one-half clock cycle long, will be output on the CNT_{DCDR} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/D pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{DCDR} pulse, and held one clock cycle after the rising edge of the CNT_{DCDR} pulse. These outputs are not affected by the inhibit logic. See Figures 5 and 12 for detailed timing.

Cascade Output (HCTL-2020 Only)

The cascade output also consists of count and up/down outputs. When the HCTL-2020 internal counter overflows or underflows, a pulse, one-half clock cycle long, will be output on the CNT_{CAS} pin. This output will occur during the clock cycle in which the internal counter is updated. The $U/\overline{D}$ pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{CAS} pulse, and held one clock cycle after the rising edge of the CNT_{CAS} pulse. These outputs are not affected by the inhibit logic. See Figures 5 and 12 for detailed timing.

Step	SEL	$\overline{OE}$	CLK	Inhibit Signal	Action
1	L	L	⌊	1	Set inhibit; read high byte
2	H	L	⌊	1	Read low byte; starts reset
3	X	H	⌊	0	Completes inhibit logic reset

Figure 10. Two Byte Read Sequence.

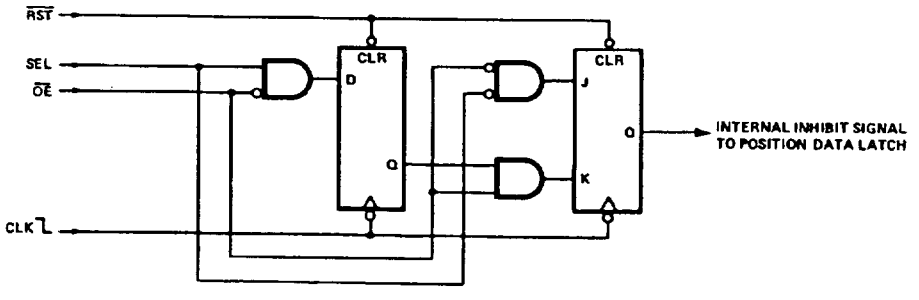


Figure 11. Simplified Inhibit Logic.

intersil

AD7545

August 1997

12-Bit, Buffered, Multiplying CMOS DAC

Features

- 12-Bit Resolution
- Low Gain T.C. 2ppm/°C (Typ)
- Fast TTL/CMOS Compatible Data Latches
- Single +5V to +15V Supply
- Low Power
- Low Cost
- /883 Processed Versions Available

Description

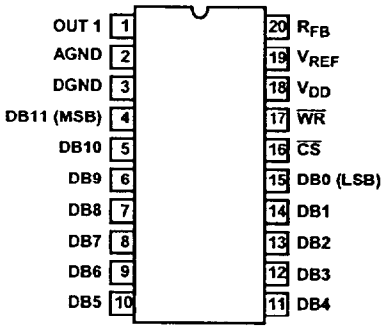
The AD7545 is a low cost monolithic 12-bit, CMOS multiplying DAC with on-board data latches. Data is loaded in a single 12-bit wide word which allows interfacing directly to most 12-bit and 16-bit bus systems. Loading of the input latches is under the control of the CS and WR inputs. A logic low on these control inputs makes the input latches transparent allowing direct unbuffered operation of the DAC.

Ordering Information

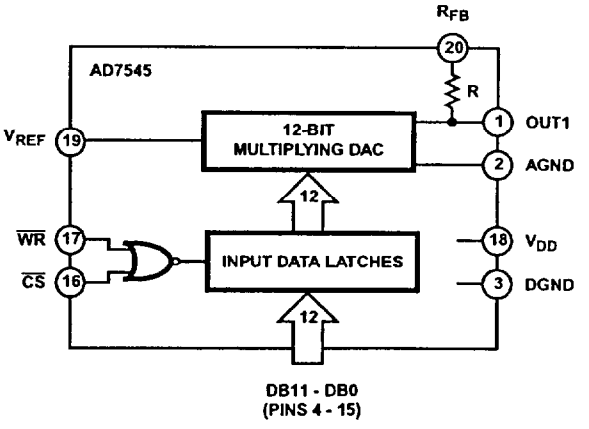
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD7545JN	0 to 70	20 Ld PDIP	E20.3
AD7545KN	0 to 70	20 Ld PDIP	E20.3
AD7545AN	-40 to 85	20 Ld PDIP	E20.3
AD7545BN	-40 to 85	20 Ld PDIP	E20.3

Pinout

AD7545
(PDIP)
TOP VIEW



Functional Diagram



File Number 3108.1

Absolute Maximum Ratings

Supply Voltage (V_{DD} to DGND) ..... -0.3V, +17V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND ..... ±25V
V_{PIN1} to DGND ..... -0.3V, V_{DD} +0.3V
AGND to DGND ..... -0.3V, V_{DD} +0.3V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	125

Maximum Junction Temperature (PDIP Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

Operating Conditions

Temperature Ranges
Commercial (J, K, Grades) ..... 0°C to 70°C
Industrial (A, B, Grades) ..... -40°C to 85°C
Extended (S Grades) ..... -55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = See Note 2, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	V_{DD} = +5V			V_{DD} = +15V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution			12			12			Bits
Relative Accuracy	J, A, S		-	-	±2	-	-	±2	LSB
	K, B		-	-	±1	-	-	±1	LSB
Differential Nonlinearity	J, A, S	10-Bit Monotonic T_{MIN} to T_{MAX}	-	-	±4	-	-	±4	LSB
	K, B	12-Bit Monotonic T_{MIN} to T_{MAX}	-	-	±1	-	-	±1	LSB
Gain Error (Using Internal RFB)	J, A, S	DAC Register Loaded with 1111 1111 1111	-	-	±20	-	-	±25	LSB
	K, B	Gain Error is Adjustable Using the Circuits of Figures 4 and 5 (Note 3)	-	-	±10	-	-	±15	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature		Typical Value is 2ppm/°C for V_{DD} = +5V (Note 4)	-	-	±5	-	-	±10	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD}		ΔV_{DD} = ±5%	0.015	-	0.03	0.01	-	0.02	%
Output Leakage Current at OUT1	J, K	DB0 - DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V (Note 2)	-	-	50	-	-	50	nA
	A, B		-	-	50	-	-	50	nA
	S		-	-	200	-	-	200	nA
DYNAMIC CHARACTERISTICS									
Current Setting Time		To $^1/_2$ LSB, OUT1 LOAD = 100Ω, DAC Output Measured from Falling Edge of $\overline{WR}$, $\overline{CS}$ = 0V (Note 4)	-	-	2	-	-	2	µs
Propagation Delay from Digital Input Change to 90% of Final Analog Output		OUT1 LOAD = 100Ω, C_{EXT} = 13pF (Notes 4 and 5)	-	-	300	-	-	250	ns
Digital to Analog Glitch Impulse		V_{REF} = AGND	-	400	-	-	250	-	nV/s
AC Feedthrough at OUT1		V_{REF} = ±10V, 10kHz Sinewave (Note 6)	-	5	-	-	5	-	mV_{P-P}
ANALOG OUTPUTS									
Output Capacitance C_{OUT1}		DB0 - DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V (Note 4)	-	-	70	-	-	70	pF
C_{OUT1}		DB0 - DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V (Note 4)	-	-	200	-	-	200	pF

Electrical Specifications T_A = See Note 2, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	V_{DD} = +5V			V_{DD} = +15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE INPUT								
Input Resistance (Pin 19 to GND)	Input Resistance TC = -300ppm/°C (Typ)	7	-	-	7	-	-	kΩ
	Typical Input Resistance = 11kΩ	-	-	25	-	-	25	kΩ
DIGITAL INPUTS								
Input High Voltage, V_{IH}		2.4	-	-	-	-	13.5	V
Input Low Voltage, V_{IL}		-	-	0.8	-	-	1.5	V
Input Current, I_{IN}	V_{IN} = 0 or V_{DD} (Note 7)	±1	-	±10	±1	-	±10	µA (Max)
Input Capacitance DB0 - DB11	V_{IN} = 0 (Note 4)	-	-	7	-	-	7	pF
$\overline{WR}$, $\overline{CS}$	V_{IN} = 0 (Note 4)	-	-	20	-	-	20	pF
SWITCHING CHARACTERISTICS (Note 4)								
Chip Select to Write Setup Time, t_{CS}	See Figure 1	380	200	-	200	120	-	ns
Chip Select to Write Hold Time, t_{CH}	See Figure 1	0	-	-	0	-	-	ns
Write Pulse Width, t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$, See Figure 1	400	175	-	240	100		ns
Data Setup Time, t_{DS}	See Figure 1	210	100	-	120	60	-	ns
Data Hold Time, t_{DH}	See Figure 1	10	-	-	10	-	-	ns
POWER SUPPLY CHARACTERISTICS								
I_{DD}	All Digital Inputs V_{IL} or V_{IH}	-	-	2	-	-	2	mA
	All Digital Inputs 0V or V_{DD}	-	100	500	-	100	500	µA
	All Digital Inputs 0V or V_{DD}	-	10	-	-	10	-	µA

NOTES:

2. Temperature Ranges as follows: J, K versions: 0°C to 70°C
   A, B versions: -20°C to 85°C
   S version: -55°C to 125°C
   T_A = 25°C for TYP Specifications. MIN and MAX are measured over the specified operating range.
3. This includes the effect of 5ppm maximum gain TC.
4. Parameter not tested. Parameter guaranteed by design, simulation, or characterization.
5. DB0 - DB11 = 0V to V_{DD} or V_{DD} to 0V in plastic and sidebraze package.
6. Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.
7. Logic inputs are MOS gates. Typical input current (25°C) is less than 1nA.
8. Typical values are not guaranteed but reflect mean performance specification.
   Specifications subject to change without notice.

Timing Diagrams

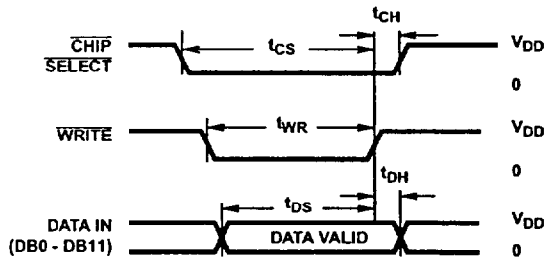


FIGURE 1A. TYPICAL WRITE CYCLE

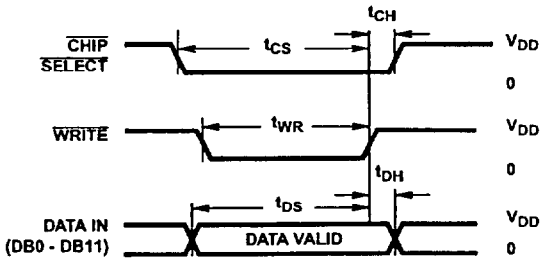


FIGURE 1B. PREFERRED WRITE CYCLE

FIGURE 1. WRITE CYCLE TIMING DIAGRAM

MODE SELECTION	
WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0 - DB11) inputs	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0 - DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:

9. V_{DD} = +5V; $t_r = t_f$ = 20ns
10. V_{DD} = +15V; $t_r = t_f$ = 40ns
11. All input signal rise and fall times measured from 10% to 90% of V_{DD}.
12. Timing measurement reference level is $(V_{IH} + V_{IL})/2$.
13. Since input data latches are transparent for $\overline{CS}$ and $\overline{WR}$ both low, it is preferred to have data valid before $\overline{CS}$ and $\overline{WR}$ both go low. This prevents undesirable changes at the analog output while the data inputs settle.

Circuit Information - D/A Converter Section

Figure 2 shows a simplified circuit of the D/A converter section of the AD7545. Note that the ladder termination resistor is connected to AGND. R is typically 11kΩ.

The binary weighted currents are switched between the OUT1 bus line and AGND by N-Channel switches, thus maintaining a constant current in each ladder leg independent of the switch state. One of the current switches is shown in Figure 3.

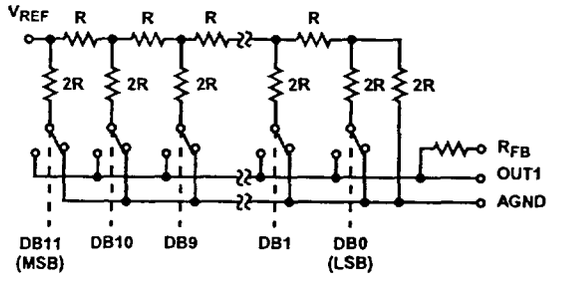


FIGURE 2. SIMPLIFIED D/A CIRCUIT OF AD7545

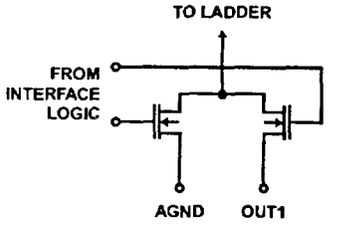


FIGURE 3. N-CHANNEL CURRENT STEERING SWITCH

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 200pF (all switches to OUT1).

The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to the value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor).

Circuit Information - Digital Section

Figure 4 shows the digital structure for one bit. The digital signals CONTROL and $\overline{CONTROL}$ are generated from $\overline{CS}$ and $\overline{WR}$.

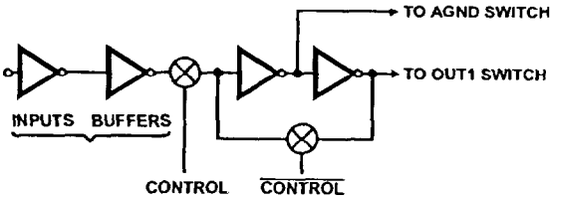


FIGURE 4. DIGITAL INPUT STRUCTURE

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0V to 3.5V the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range 5V ≤ V_{DD} ≤ 15V. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

Application

Output Offset

CMOS current-steering D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation.

General Ground Management

AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND connection is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches

When $\overline{WR}$ and $\overline{CS}$ are both low the latched are transparent and the D/A converter inputs follow the data inputs. In some

bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse ($\overline{WR}$) so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by isolating the analog pins of the AD7545 (pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid isolation at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5V. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induces noise.

Temperature Coefficients

The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account.

Basic Applications

Figures 5 and 6 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that the circuits of Figures 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0V to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an AC signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20V \le V_{IN} \le +20V$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 4.

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive -OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

The choice of the operational amplifiers in Figure 4 and Figure 5 depends on the application and the trade off between required precision and speed. Below is a list of operational amplifiers which are good candidates for many applications. The main selection criteria for these operational amplifiers is to have low V_{OS}, low V_{OS} drift, low bias current and low settling time.

These amplifiers need to maintain the low nonlinearity and monotonic operation of the D/A while providing enough speed for maximum converter performance.

Operational Amplifiers

HA5127 Ultra Low Noise, Precision
HA5137 Ultra Low Noise, Precision, Wide Band
HA5147 Ultra Low Noise, Precision, High Slew Rate
HA5170 Precision, JFET Input

TABLE 1. RECOMMENDED TRIM RESISTOR VALUES vs GRADES FOR V_{DD} = +5V

TRIM RESISTOR	J, A, S	K, B
R1	500Ω	200Ω
R2	150Ω	68Ω

TABLE 2. UNIPOLAR BINARY CODE TABLE FOR CIRCUIT OF FIGURE 5

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -\frac{1}{2}V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0V

TABLE 3. 2'S COMPLEMENT CODE TABLE FOR CIRCUIT OF FIGURE 6

DATA INPUT			ANALOG OUTPUT
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0V
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

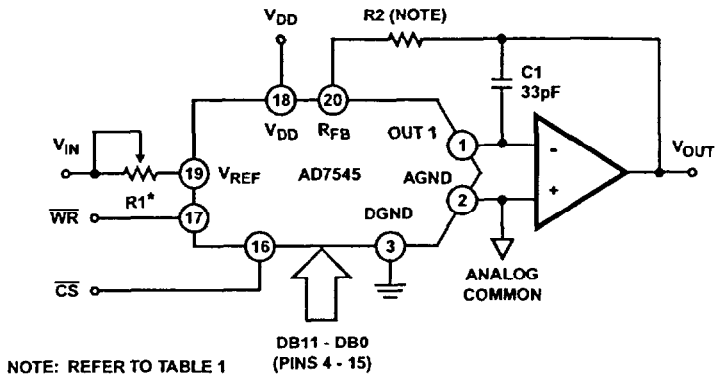


FIGURE 5. UNIPOLAR BINARY OPERATION

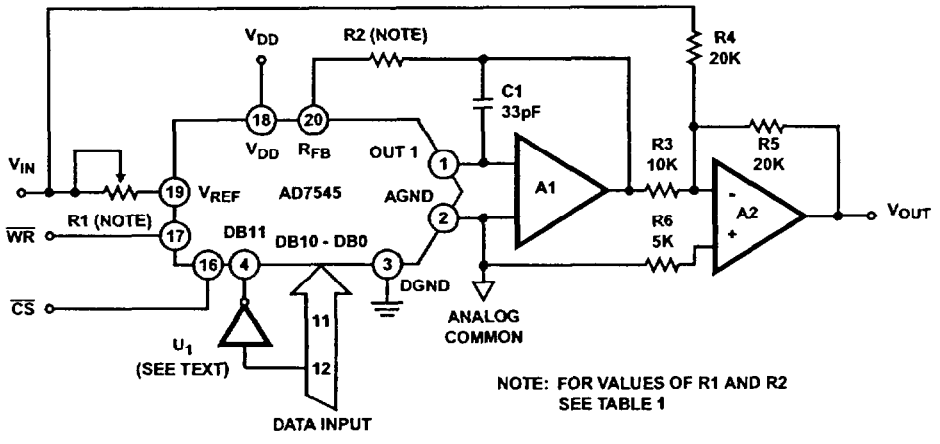


FIGURE 6. BIPOLAR OPERATION (2'S COMPLEMENT CODE)

MC6850

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

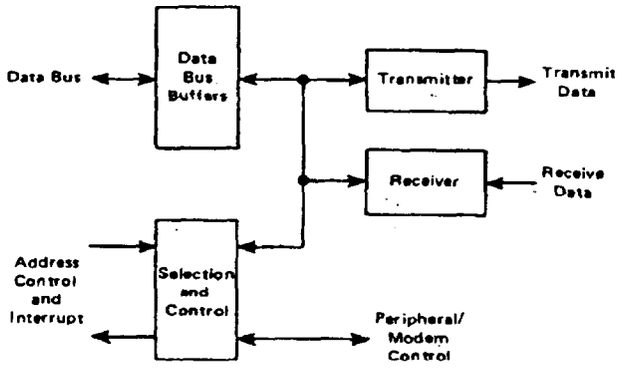
The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit-bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

- 8- and 9-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 1.0 Mbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One- or Two-Stop Bit Operation

3

MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER BLOCK DIAGRAM



MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6850, MC68A50, MC68B50 MC6850C, MC68A50C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Cerdip	θ_{JA}	 120 65	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS}+2.0	—	V_{CC}	V
Input Low Voltage		V_{IL}	V_{SS}−0.3	—	V_{SS}+0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	R/W, CS0, CS1, CS2, Enable RS, Rx D, Rx C, CTS, DCD	I_{in}	—	1.0	2.5	µA
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4 V)	D0-D7	I_{TSI}	—	2.0	10	µA
Output High Voltage (I_{Load} = −205 µA, Enable Pulse Width < 25 µs) (I_{Load} = −100 µA, Enable Pulse Width < 25 µs)	D0-D7 Tx Data, RTS	V_{OH}	V_{SS}+2.4 V_{SS}+2.4	— —	— —	V
Output Low Voltage (I_{Load} = 1.6 mA, Enable Pulse Width < 25 µs)		V_{OL}	—	—	V_{SS}+0.4	V
Output Leakage Current (Off State) (V_{OH} = 2.4 V)	IRQ	I_{LOH}	—	1.0	10	µA
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	—	300	525*	mW
Internal Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7 E, Tx CLK, Rx CLK, R/W, RS, Rx Data, CS0, CS1, CS2, CTS, DCD	C_{in}	— —	10 7.0	12.5 7.5	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	RTS, Tx Data IRQ	C_{out}	— —	— —	10 5.0	pF

* For temperatures less than T_A = 0°C, P_{INT} maximum will increase.

SERIAL DATA TIMING CHARACTERISTICS

Characteristic		Symbol	MC6850		MC68A50		MC68B50		Unit
			Min	Max	Min	Max	Min	Max	
Data Clock Pulse Width, Low (See Figure 1)	÷16, ÷64 Modes ÷1 Mode	PW_{CL}	600 900	– –	450 650	– –	280 500	– –	ns
Data Clock Pulse Width, High (See Figure 2)	÷16, ÷64 Modes ÷1 Mode	PW_{CH}	600 900	– –	450 650	– –	280 500	– –	ns
Data Clock Frequency	÷16, ÷64 Modes ÷1 Mode	f_C	– –	0.8 500	– –	1.0 750	– –	1.5 1000	MHz kHz
Data Clock-to-Data Delay for Transmitter (See Figure 3)		t_{TDD}	–	600	–	540	–	460	ns
Receive Data Setup Time (See Figure 4)	÷1 Mode	t_{RDS}	250	–	100	–	30	–	ns
Receive Data Hold Time (See Figure 5)	÷1 Mode	t_{RDH}	250	–	100	–	30	–	ns
Interrupt Request Release Time (See Figure 6)		t_{IR}	–	1.2	–	0.9	–	0.7	μs
Request-to-Send Delay Time (See Figure 6)		t_{RTS}	–	560	–	480	–	400	ns
Input Rise and Fall Times (or 10% of the pulse width if smaller)		t_r, t_f	–	1.0	–	0.5	–	0.25	μs

FIGURE 1 — CLOCK PULSE WIDTH, LOW-STATE

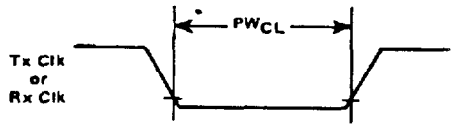


FIGURE 2 — CLOCK PULSE WIDTH, HIGH-STATE

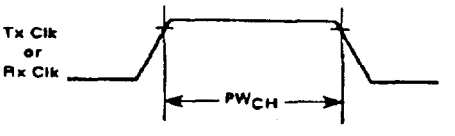


FIGURE 3 — TRANSMIT DATA OUTPUT DELAY

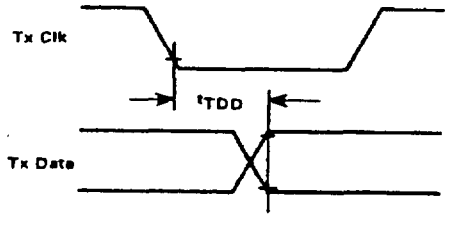


FIGURE 4 — RECEIVE DATA SETUP TIME (÷1 Mode)

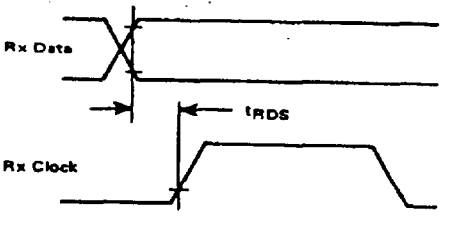


FIGURE 5 — RECEIVE DATA HOLD TIME (÷1 Mode)

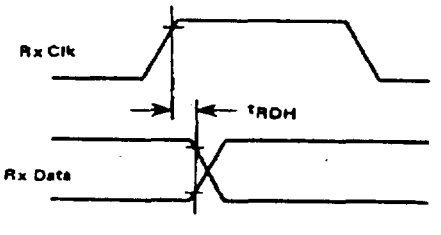
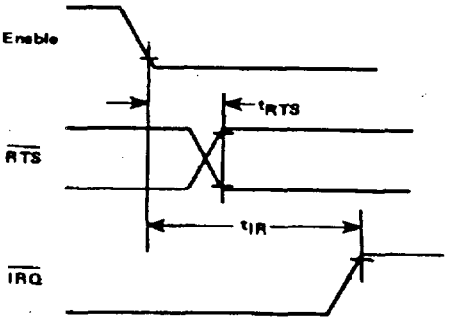


FIGURE 6 — REQUEST-TO-SEND DELAY AND INTERRUPT-REQUEST RELEASE TIMES



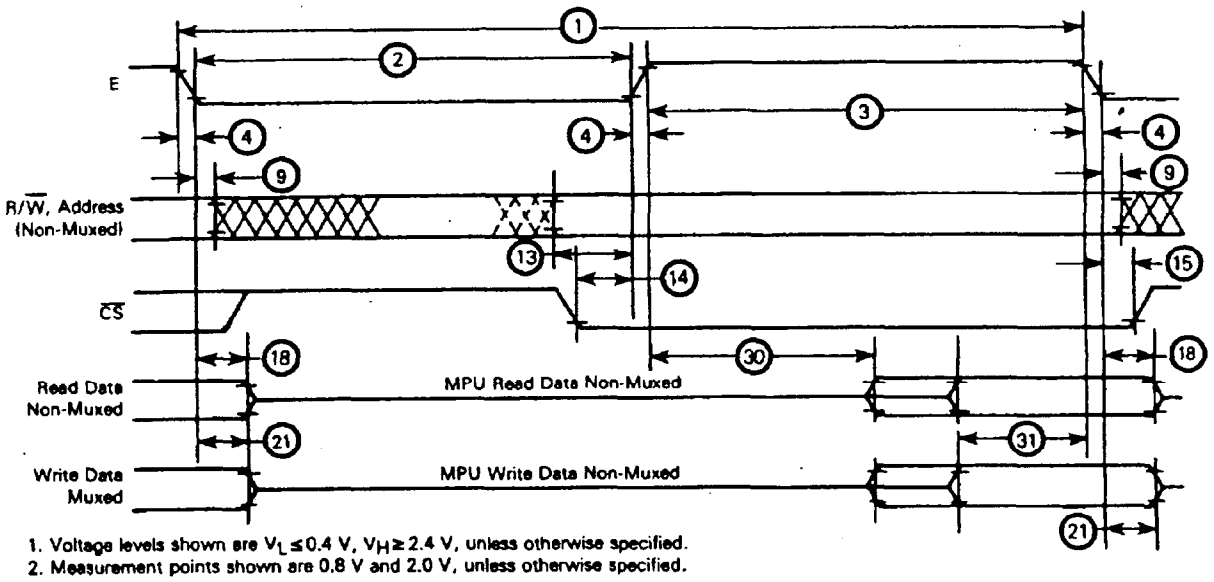
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

BUS TIMING CHARACTERISTICS (See Notes 1 and 2 and Figure 7)

Ident. Number	Characteristic	Symbol	MC6850		MC68A50		MC68B50		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	9500	280	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	220	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	10	–	10	–	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	Chip Select Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	Chip Select Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Output Data Delay Time	t_{DDR}	–	290	–	180	–	150	ns
31	Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHR}max (High Impedance).

FIGURE 7 – BUS TIMING CHARACTERISTICS



1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

FIGURE 8 – BUS TIMING TEST LOADS

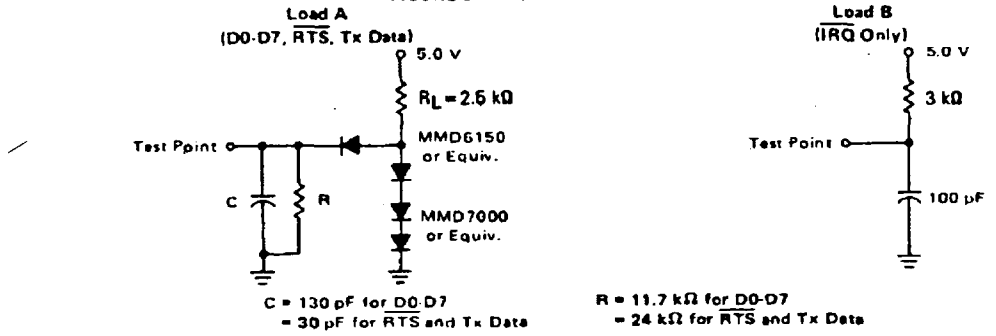
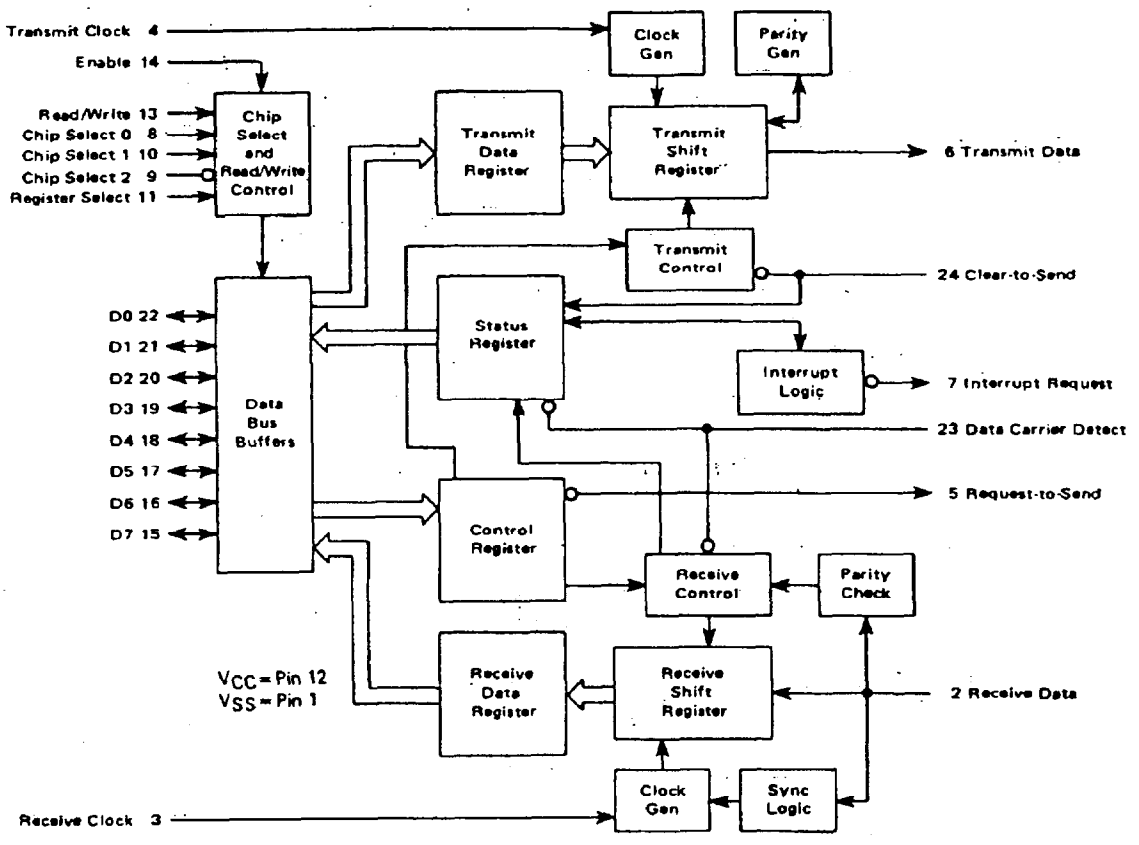


FIGURE 9 — EXPANDED BLOCK DIAGRAM



DEVICE OPERATION

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

MASTER RESET

The master reset (CR0, CR1) must be set immediately after power-up to insure the reset condition and prepare for programming the ACIA functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTS}$ outputs are held at level 1. On all other master resets, the $\overline{RTS}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. After master resetting the ACIA, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, and parity (even, odd, or none).

TRANSMIT

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even through the first character is in the process of being transmitted (because of

double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

ACIA INTERFACE SIGNALS FOR MPU

The ACIA interfaces to the M6800 MPU with an 8-bit bidirectional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the ACIA.

ACIA Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation.

ACIA Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the MC6800 $\phi 2$ Clock or MC6809 E clock.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is low, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the ACIA.

Chip Select (CS0, CS1, $\overline{CS2}$) — These three high-impedance TTL-compatible input lines are used to address the ACIA. The ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the ACIA are then performed under the control of the Enable Signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request (IRQ) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set. The IRQ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the ACIA. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•$\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the ACIA being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the ACIA. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the ACIA. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

Transmit Clock (Tx CLK) — The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (Rx CLK) — The Receive Clock input is used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (Tx Data) — The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) — This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The RTS output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

Data Carrier Detect ($\overline{DCD}$) — This high-impedance TTL-compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low-to-high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set. The Rx CLK must be running for proper $\overline{DCD}$ operation.

ACIA REGISTERS

The expanded block diagram for the ACIA indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

TABLE 1 — DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • $\overline{R/W}$ Transmit Data Register (Write Only)	RS • R/$\overline{W}$ Receive Data Register (Read Only)	$\overline{RS}$ • R/$\overline{W}$ Control Register (Write Only)	$\overline{RS}$ • R/$\overline{W}$ Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear-to-Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request (IRQ)

* Leading bit = LSB = Bit 0
** Data bit will be zero in 7-bit plus parity modes.
*** Data bit is "don't care" in 7-bit plus parity modes.