SGS-THOMSON MICROELECTRONICS

M54HC221/221A
M74HC221/221A

DUAL MONOSTABLE MULTIVIBRATOR

- HIGH SPEED
  t_{PD} = 25 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC}=4 µA (MAX.) AT T_A=25°C
  ACTIVE STATE I_{CC} = 700 µA (MAX.) AT V_{CC}=5V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OH} = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 150 ns ~ 60 s OVER AT V_{CC} = 4.5 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS221

B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

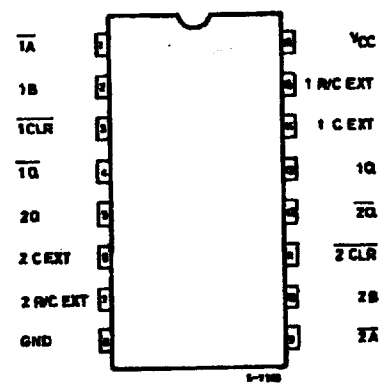
ORDER CODES :

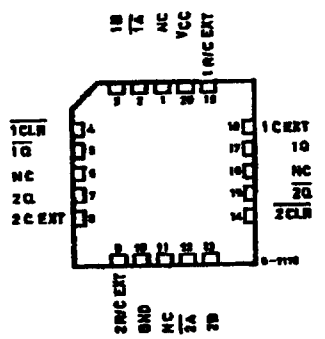
M54HCXXXF1R	M74HCXXXXM1R
M74HCXXXB1R	M74HCXXXC1R

DESCRIPTION

The M54/74HC221/221A are high speed CMOS MONOSTABLE multivibrators fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, $\overline{A}$ INPUT (negative edge) and B INPUT (positive edge). Triggering on the B input occurs at a particular voltage threshold and is not related to the rise and fall time of the applied pulse. The device may also be triggered by using the $\overline{CLR}$ input (positive-edge) because of the Schmitt-trigger input ; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx. Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer.
Limit for values of Cx and Rx :
Cx : NO LIMIT
Rx : V_{CC} < 3.0 V 5 K Ω to 1 M Ω
V_{CC} ≥ 3.0 V 1 K Ω to 1 M Ω
Two different pulse width constants are available:
K ≅ 0.7 for HC221
K ≅ 1 for HC221A
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

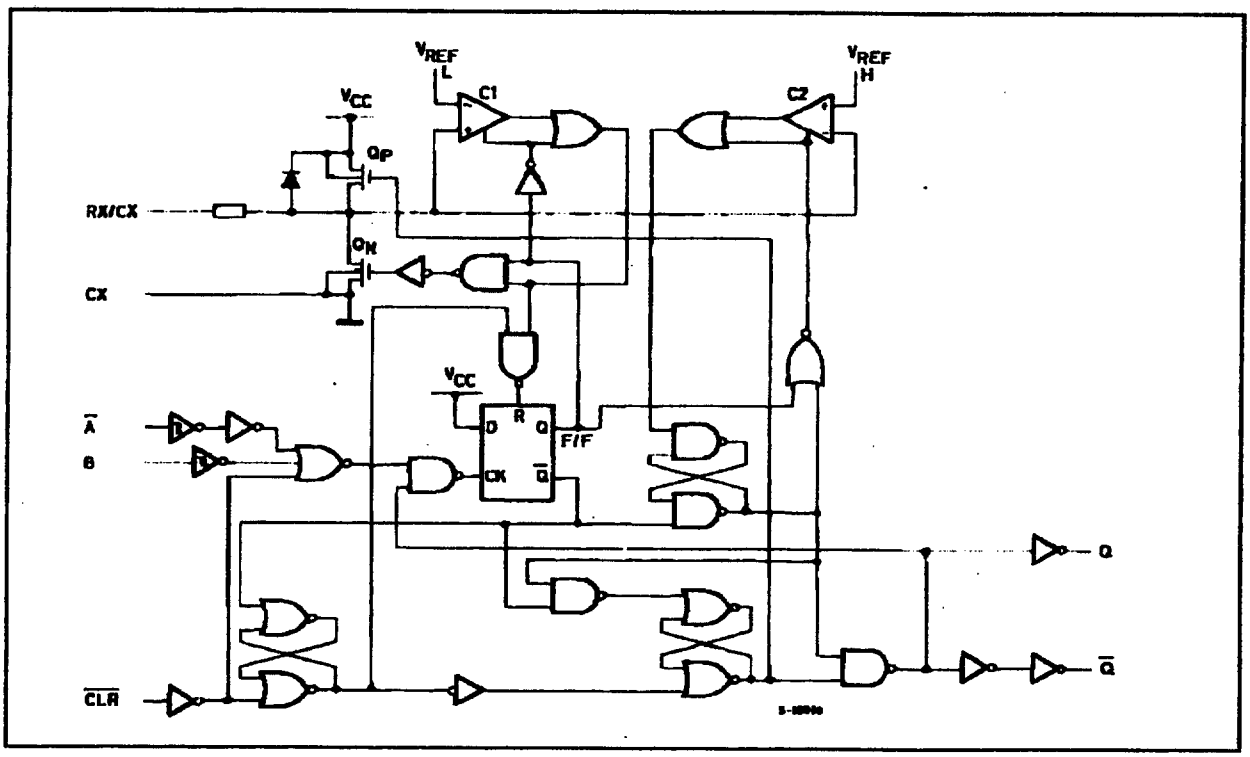
PIN CONNECTIONS (top view)



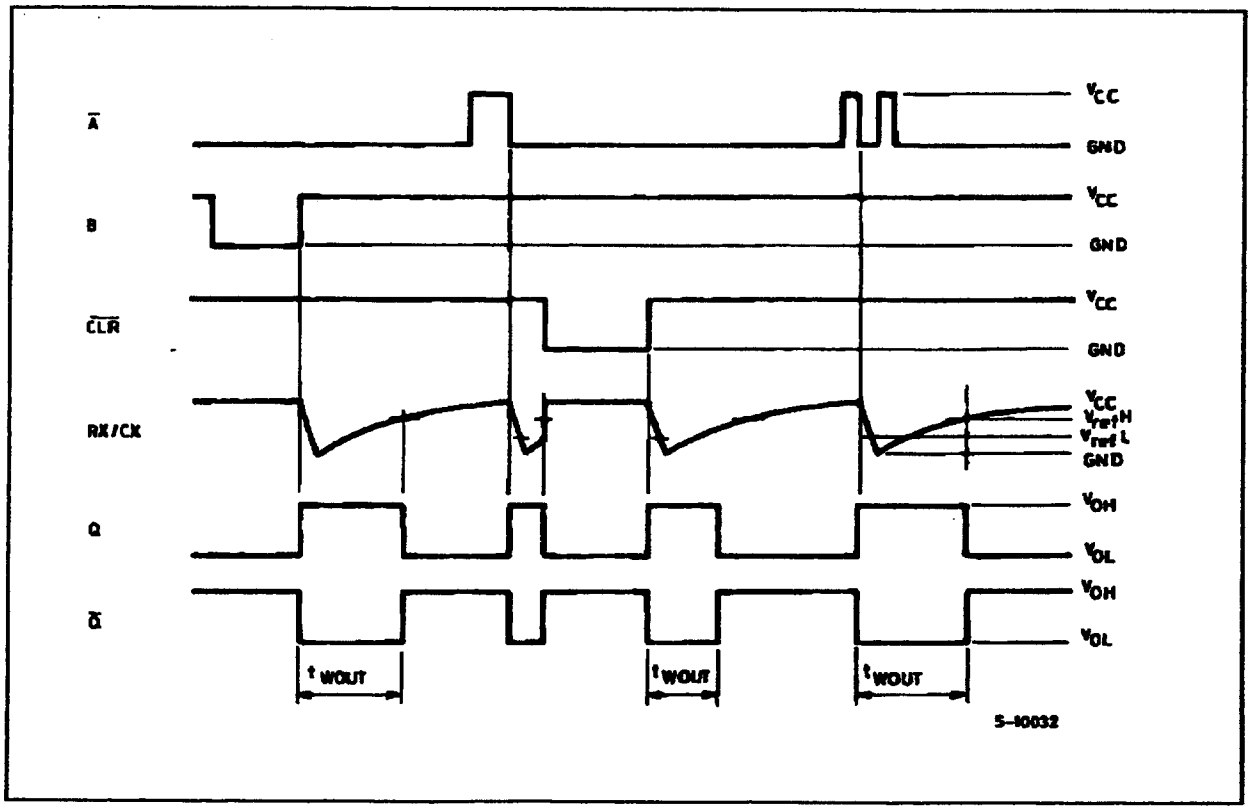


NC =
No Internal
Connection

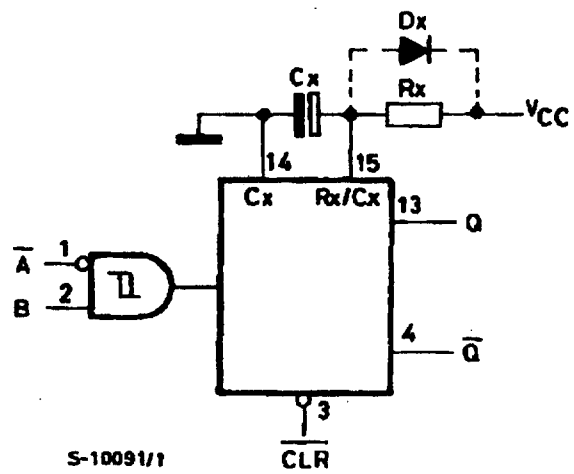
SYSTEM DIAGRAM

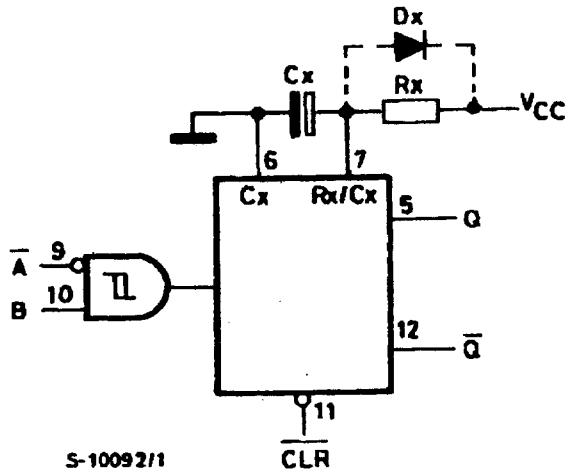


TIMING CHART



BLOCK DIAGRAM





Note :

(1) Cx, Rx, Dx are external components.

(2) Dx is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidly, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows :

$t_f \geq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when :

1st) A is "low" and B has a falling edge ;
2nd) B is "high" and A has a rising edge ;
3rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node R/C external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.

At this point C1 stops functioning but C2 continues to operate.

The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and O goes low. C2 stop operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx · Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows :

$$t_{W(OUT)} = 0.70\ Cx \cdot Rx\ (HC221)$$

$$t_{W(OUT)} = Cx \cdot Rx\ (HC221A)$$

RESET OPERATION

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

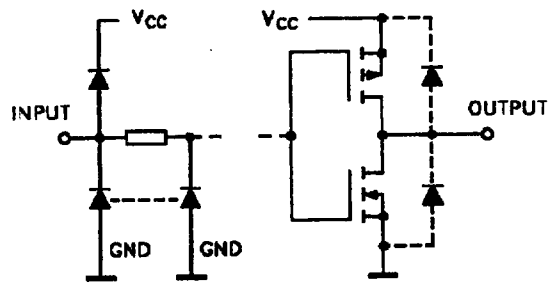
Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
⌐	H	H	⌐¯	¯⌐	OUTPUT ENABLE
X	L	H	L (*)	H (*)	INHIBIT
H	X	H	L (*)	H (*)	INHIBIT
L	⌐	H	⌐¯	¯⌐	OUTPUT ENABLE
L	H	⌐	⌐¯	¯⌐	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: Don't Care (*): Except for monostble period

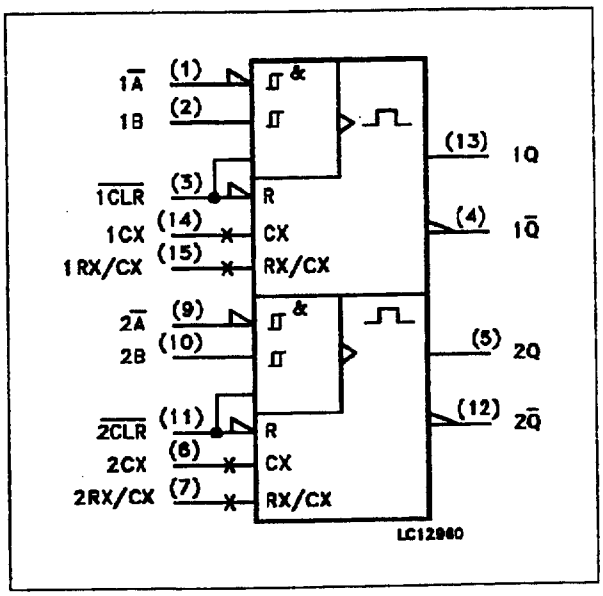
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	Trigger Inputs (Negative Edge Triggered)
2, 10	1B, 2B	Trigger Inputs (Positive Edge Triggered)
3, 11	$1\overline{CLR}$, $2\overline{CLR}$	Direct Reset LOW and Trigger Action at Positive Edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	Outputs (Active LOW)
7	$2R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
13, 5	1Q, 2Q	Outputs (Active HIGH)
14, 6	$1C_{EXT}$ $2C_{EXT}$	External Capacitor Connection
15	$1R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



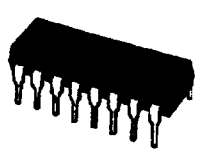
SGS-THOMSON MICROELECTRONICS

HCC4020B/24B/40B
HCF4020B/24B/40B

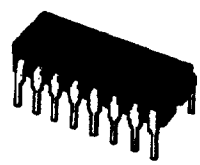
RIPPLE-CARRY BINARY COUNTER/DIVIDERS

4020B - 14 STAGE
4024B - 7 STAGE
4040B - 12 STAGE

- MEDIUM-SPEED OPERATION
- FULLY STATIC OPERATION
- COMMON RESET
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT
- CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)



F
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES:

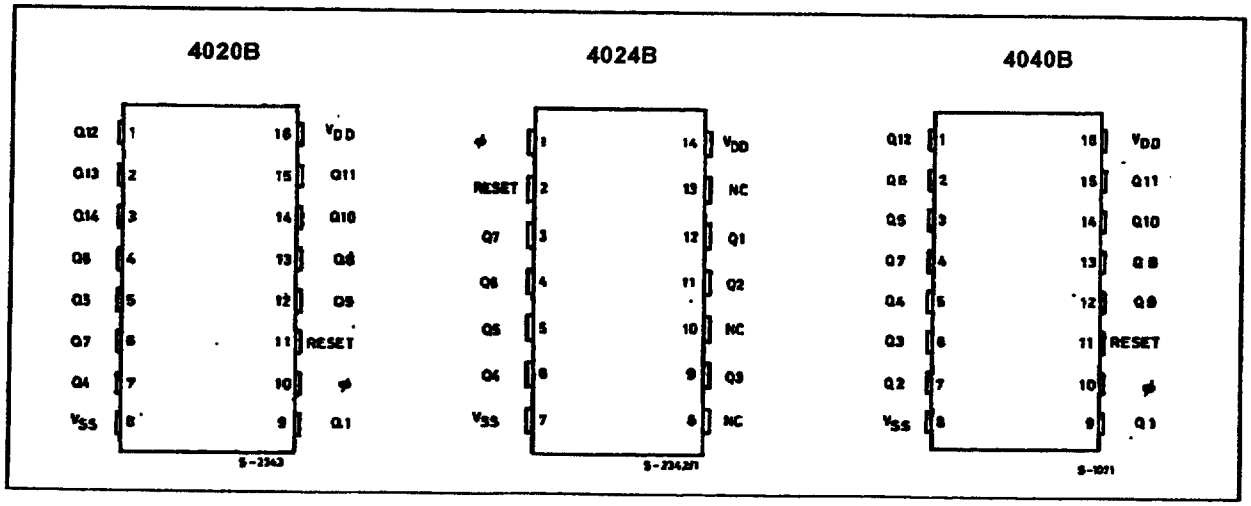
HCC40XXBF HCF40XXBM1
HCF40XXBEY HCF40XXBC1

DESCRIPTION

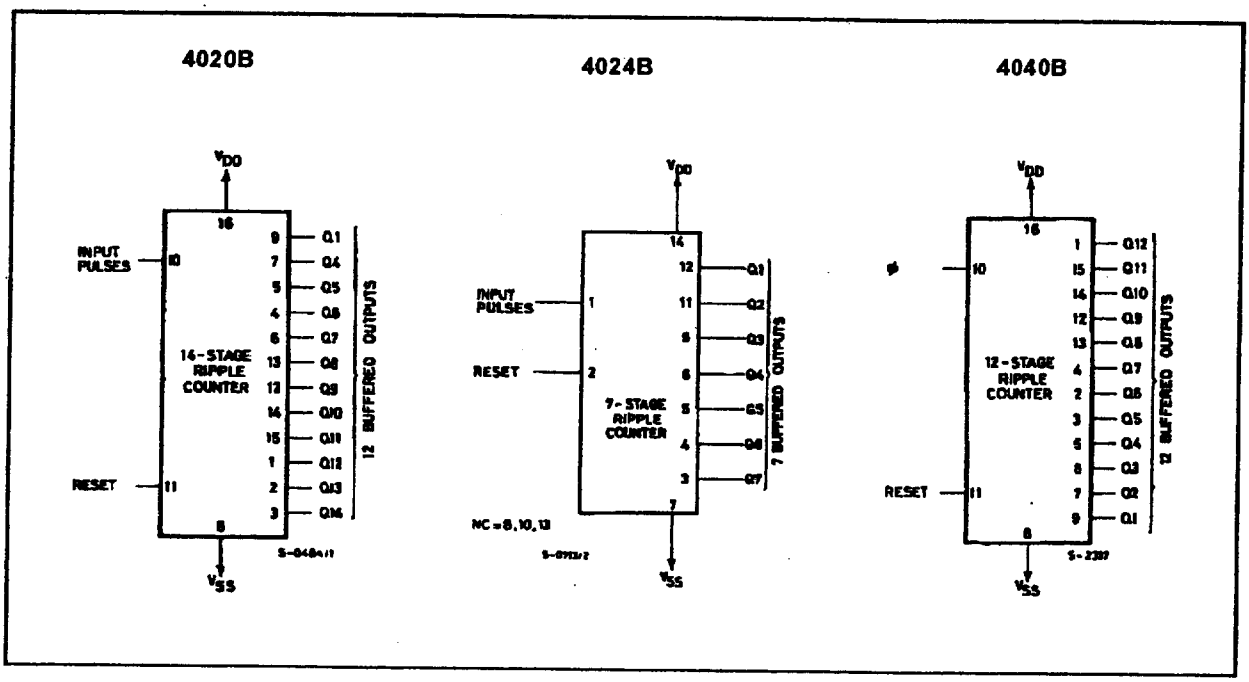
The **HCC4XXXB** (extended temperature range) and **HCF4XXXB** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line for **4024B** and 16-lead dual in-line for **4020B, 4040B** plastic or ceramic package and plastic micropackage.

The **HCC/HCF4020B, 4024B**, and **4040B** are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse ; a high level on the RESET line resets the counter to its all zeros stage. Schmitt trigger action on the input-pulse line permits unlimited clock rise and fall times. All inputs and outputs are buffered.

PIN CONNECTIONS



FUNCTIONAL DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : HCC Types HCF Types	− 0.5 to + 20 − 0.5 to + 18	V V
V_I	Input Voltage	− 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : HCC Types HCF Types	− 55 to + 125 − 40 to + 85	°C °C
T_{stg}	Storage Temperature	− 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are refered to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : HCC Types HCF Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : HCC Types HCF Types	− 55 to + 125 − 40 to + 85	°C °C

National Semiconductor

March 1988

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BM/CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BM/CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BM/CD4017BC and CD4022BM/CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

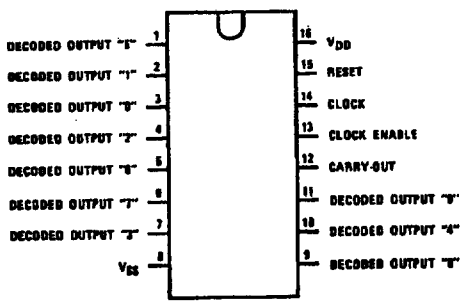
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	5.0 MHz (typ.) with 10V V_{DD}
■ Low power	10 μW (typ.)
■ Fully static operation	

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

Connection Diagrams

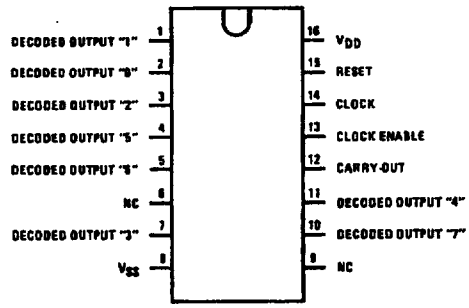
CD4017B
Dual-In-Line Package



TL/F/5950–1

Top View

CD4022B
Dual-In-Line Package



TL/F/5950–2

Top View

Order Number CD4017B or CD4022B

RRD-B30M105/Printed in U. S. A.

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

AC Electrical Characteristics*

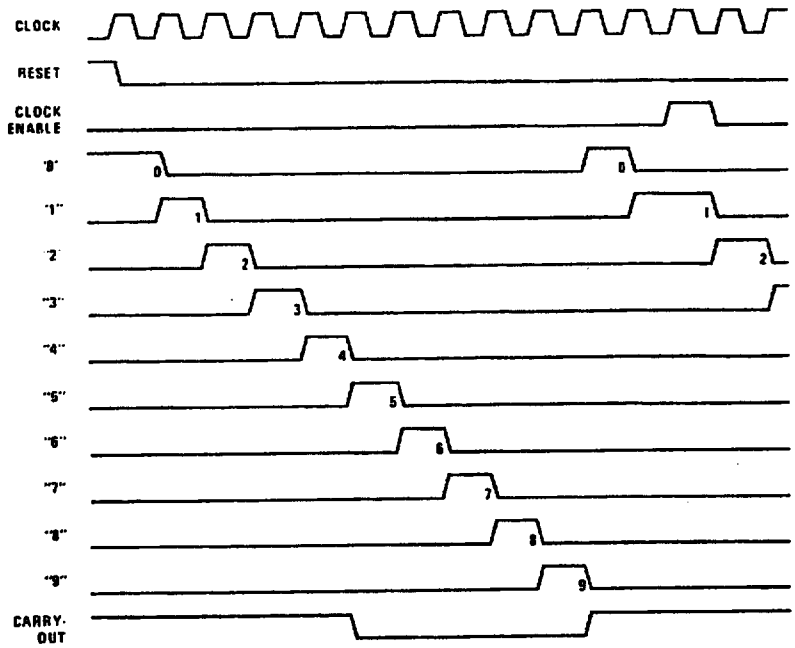
T_A = 25°C, C_L = 50 pF, R_L = 200k, t_{rCL} and t_{fCL} = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry Out Line	V_{DD} = 5V		415	800	ns
		V_{DD} = 10V		160	320	ns
		V_{DD} = 15V		130	250	ns
	Carry Out Line	V_{DD} = 5V, C_L = 15 pF		240	480	ns
		V_{DD} = 10V, C_L = 15 pF		85	170	ns
		V_{DD} = 15V, C_L = 15 pF		70	140	ns
	Decode Out Lines	V_{DD} = 5V		500	1000	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_W	Minimum Reset Pulse Width	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
t_{REM}	Minimum Reset Removal Time	V_{DD} = 5V		75	150	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns

*AC Parameters are guaranteed by DC correlated testing.

Timing Diagrams

CD4017B



TL/F/5950–3