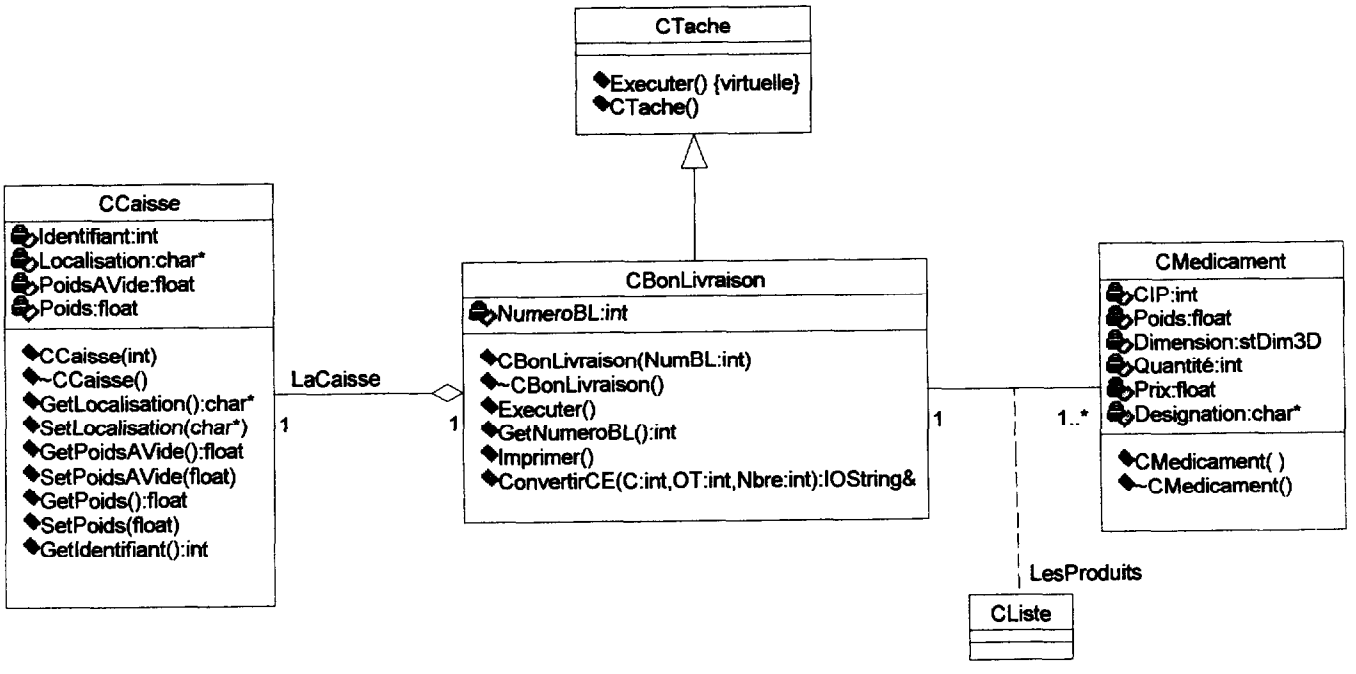
Annexes du sujet

Diagramme de classe (extrait)



Le schéma logique de la base de données relationnelle est le suivant :

CLIENT(N°client, Nom, Rue, CodePostal, Ville, Tel)
MEDICAMENT(CIP, Désignation, Dim_Hauteur, Dim_Largeur, Dim_Longueur, Poids, Prix, Quantité)
ZONEATELIER(N°zone, CodeGéo)
COMMANDE(#N°client,#CIP,Date)
LOCALISER(#N°zone, #CIP)

Nous allons donner un exemple de contenu des relations (ou tables) MEDICAMENT, ZONEATELIER et LOCALISER.

La relation MEDICAMENT :

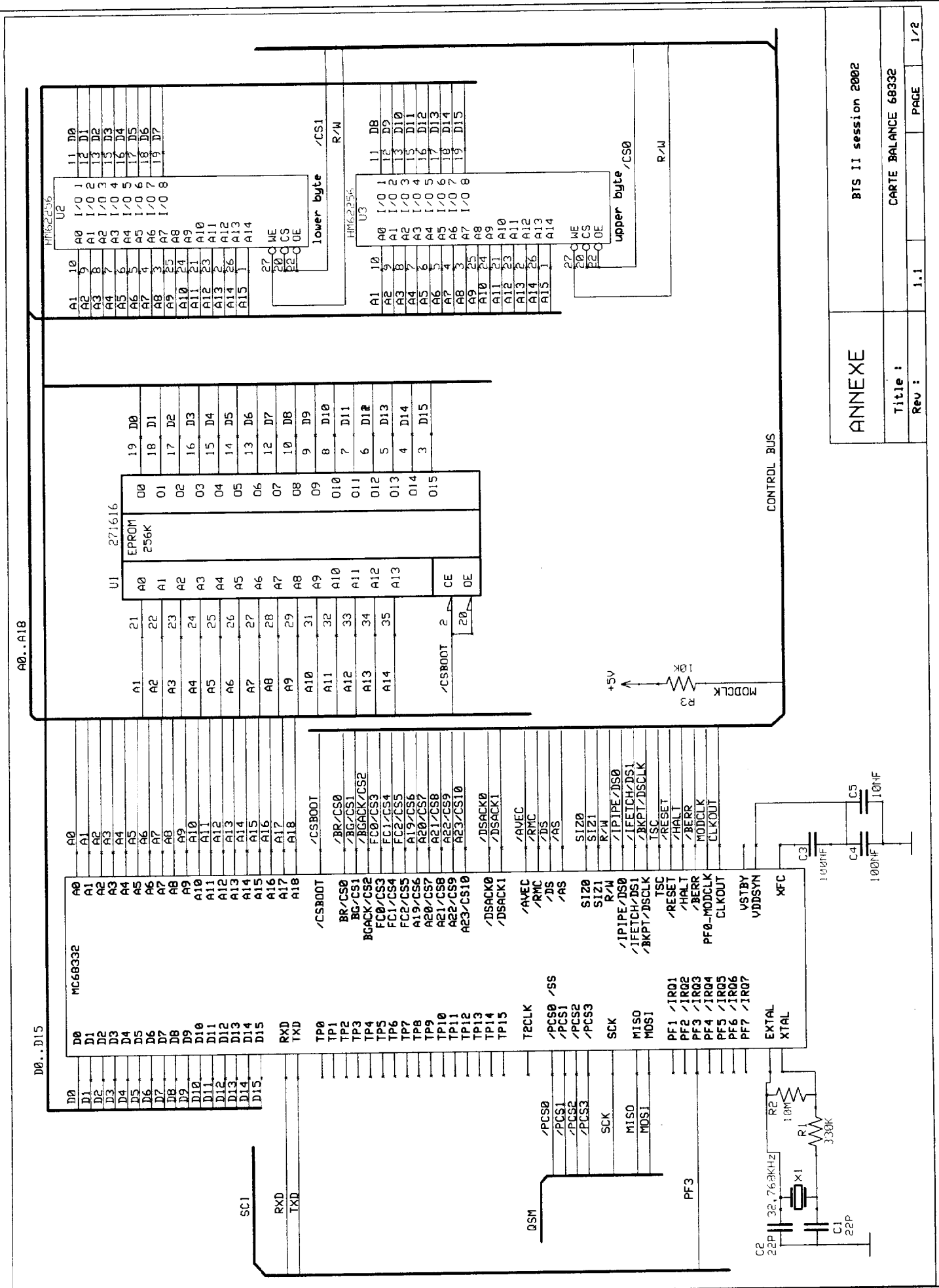
CIP	Désignation	Hauteur	Largeur	Longueur	Poids	Prix	Quantité
3153359	TEMESTA CPR 1MG50	65	45	60	20	****	1500
3213593	COLPOSEPTINE CPR GYNECO 18	20	60	130	37	****	2000
3236252	ELASE POM T 20G GM	30	30	1400	32	****	1250
3254971	VARNOLINE CPR 21	40	35	70	12	****	1120
3278457	NOROXINE 400MG CPR 10	15	42	95	13	****	2310
3299063	TANAKAN CPR 90	17	17	62	47	****	3010
3326357	LIPANTHYL 200 MICRONIS GELU 30	25	60	90	26	****	780
3349571	LAMISIL 250MG CPR SECB BT 28	20	38	95	22	****	650
3512545	ALDACTONE 75MG CPR BT 30	27	42	98	17	****	1789

La relation ZONEATELIER :

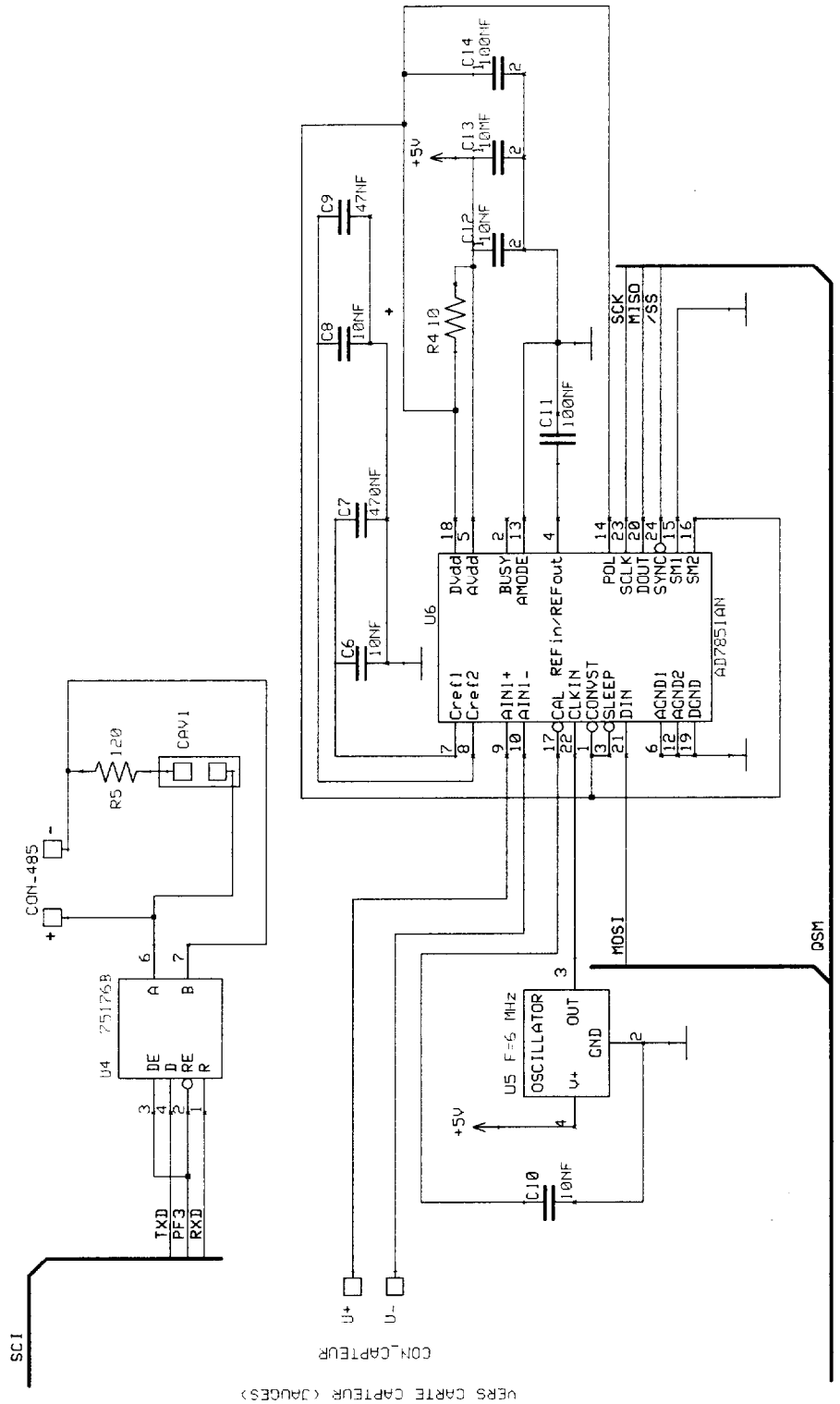
N°zone	CodeGéo
1	10000
2	10001
3	20003
4	22000
5	12019
6	20133
7	11836
8	11600
9	21515
10	120324

La relation LOCALISER :

#CIP	#N°zone
3153359	1
3153359	6
3153359	3
3153359	9
3213593	2
3213593	4
3326357	5
3326357	7
3326357	8
3326357	10


ANNEXE
BTS II session 2002
CARTE BALANCE 68332
Title :
Rev : 1.1
PAGE 1/2
U1 27C1616 EPROM 256K
U2 HM62256 lower byte
U3 HM62256 upper byte
MC68332
CONTROL BUS
A0..A18
D0..D15
/CS0
/CS1
R/W
/CSBOOT
MODCLK
+5V
10K
R3
R1 330K
R2 10M
X1 32.768KHz
C1 22P
C2 22P
C3 100NF
C4 100NF
C5 10NF
SCI
RXD
TXD
QSM
SCK
MISO
MOSI
PF3

ANNEXE	BTS II session 2002	
	CARTE BALANCE 68332	
Title :		PAGE 2/2
Rev :	1.1	



ANALOG DEVICES

14-Bit 333 kSPS Serial A/D Converter

AD7851

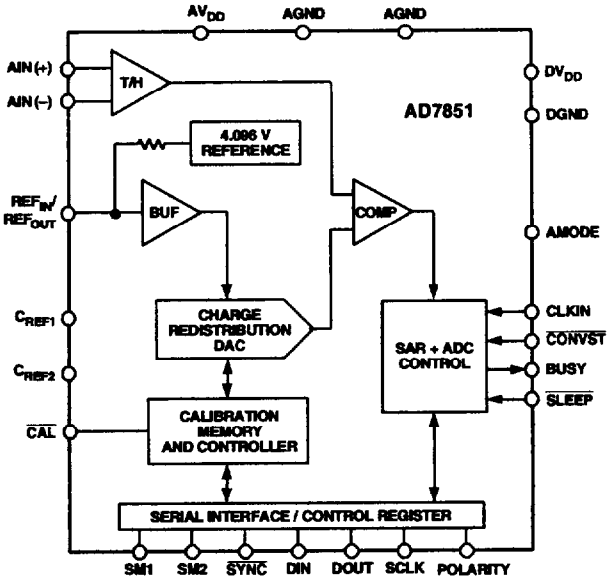
FEATURES

Single 5 V Supply
333 kSPS Throughput Rate/±2 LSB DNL—A Grade
285 kSPS Throughput Rate/±1 LSB DNL—K Grade
A & K Grades Guaranteed to 125°C/238 kSPS Throughput Rate
Pseudo-Differential Input with Two Input Ranges
System and Self-Calibration with Autocalibration on Power-Up
Read/Write Capability of Calibration Data
Low Power: 60 mW typ
Power-Down Mode: 5 µW typ Power Consumption
Flexible Serial Interface:
8051/SPI/QSPI/ µP Compatible
24-Pin DIP, SOIC and SSOP Packages

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control
Instrumentation and Control Systems
High Speed Modems
Automotive

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7851 is a high speed, 14-bit ADC that operates from a single 5 V power supply. The ADC powers-up with a set of default conditions at which time it can be operated as a read-only ADC. The ADC contains self-calibration and system-calibration options to ensure accurate operation over time and temperature and has a number of power-down options for low power applications.

The AD7851 is capable of 333 kHz throughput rate. The input track-and-hold acquires a signal in 0.33 µs and features a pseudo-differential sampling scheme. The AD7851 has the added advantage of two input voltage ranges (0 V to V_{REF}, and $-V_{REF}/2$ to $+V_{REF}/2$ centered about $V_{REF}/2$). Input signal range is to V_{DD} and the part is capable of converting full-power signals to 20 MHz.

CMOS construction ensures low power dissipation (60 mW typ) with power-down mode (5 µW typ). The part is available in 24-pin, 0.3 inch-wide dual-in-line package (DIP), 24-lead small outline (SOIC) and 24-lead small shrink outline (SSOP) packages.

***Patent pending.**
See Page 35 for data sheet Index.

PRODUCT HIGHLIGHTS

1. Single 5 V supply.
2. Operates with reference voltages from 4 V to V_{DD}.
3. Analog input ranges from 0 V to V_{DD}.
4. System and self-calibration including power-down mode.
5. Versatile serial I/O port.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD7851

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	$\overline{\text{CONVST}}$	starts conversion. When this input is not used, it should be tied to DV_{DD}.
2	BUSY	Busy Output. The busy output is triggered high by the falling edge of $\overline{\text{CONVST}}$ or rising edge of $\overline{\text{CAL}}$, and remains high until conversion is completed. BUSY is also used to indicate when the AD7851 has completed its on-chip calibration sequence.
3	$\overline{\text{SLEEP}}$	Sleep Input/Low Power Mode. A logic 0 initiates a sleep and all circuitry is powered down including the internal voltage reference provided there is no conversion or calibration being performed. Calibration data is retained. A logic 1 results in normal operation. See Power-Down section for more details.
4	REF_{IN} REF_{OUT}	reference source for the analog-to-digital converter. The nominal reference voltage is 4.096 V and this appears at the pin. This pin can be overdriven by an external reference or can be taken as high as AV_{DD}. When this pin is tied to AV_{DD}, then the C_{REF1} pin should also be tied to AV_{DD}.
5	AV_{DD}	Analog Positive Supply Voltage, +5.0 V 5%.
6, 12	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
7	C_{REF1}	Reference Capacitor (0.01 F ceramic disc in parallel with a 470 nF NPO type). This external capacitor is used as a charge source for the internal DAC. The capacitor should be tied between the pin and AGND.
8	C_{REF2}	Reference Capacitor (0.01 F ceramic disc in parallel with a 470 nF NPO type). This external capacitor is used in conjunction with the on-chip reference. The capacitor should be tied between the pin and AGND.
9	AIN(+)	Analog Input. Positive input of the pseudo-differential analog input. Cannot go below AGND or above AV_{DD} at any time, and cannot go below AIN(–) when the unipolar input range is selected.
10	AIN(–)	Analog Input. Negative input of the pseudo-differential analog input. Cannot go below AGND or above AV_{DD} at any time.
11	NC	No Connect Pin.
13	AMODE	Analog Mode Pin. This pin allows two different analog input ranges to be selected. A logic 0 selects range 0 to V_{REF} (i.e., AIN(+) – AIN(–) = 0 to V_{REF}). In this case AIN(+) cannot go below AIN(–) and AIN(–) cannot go below AGND. A logic 1 selects range $-V_{REF}/2$ to $+V_{REF}/2$ (i.e., AIN(+) – AIN(–) = $-V_{REF}/2$ to $+V_{REF}/2$). In this case AIN(+) cannot go below AGND so that AIN(–) needs to be biased to $+V_{REF}/2$ to allow AIN(+) to go from 0 V to $+V_{REF}$ V.
14	POLARITY	Serial Clock Polarity. This pin determines the active edge of the serial clock (SCLK). Toggling this pin will reverse the active edge of the serial clock (SCLK). A logic 1 means that the serial clock (SCLK) idles high and a logic 0 means that the serial clock (SCLK) idles low. It is best to refer to the timing diagrams and Table X for the SCLK active edges.
15	SM1	Serial Mode Select Pin. This pin is used in conjunction with the SM2 pin to give different modes of operation as described in Table XI.
16	SM2	Serial Mode Select Pin. This pin is used in conjunction with the SM1 pin to give different modes of operation as described in Table XI.
17	$\overline{\text{CAL}}$	Calibration Input. This pin has an internal pull-up current source of 0.15 A. A logic 0 on this pin resets all logic and initiates a calibration on its rising edge. There is the option of connecting a 10 nF capacitor from this pin to AGND to allow for an automatic self calibration on power-up. This input overrides all other internal operations.
18	DV_{DD}	Digital Supply Voltage, +5.0 V 5%.
19	DGND	Digital Ground. Ground reference point for digital circuitry.
20	DOUT	Serial Data Output. The data output is supplied to this pin as a 16-bit serial word.
21	DIN	Serial Data Input. The data to be written is applied to this pin in serial form (16-bit word). This pin can act as an input pin or as a I/O pin depending on the serial interface mode the part is in (see Table XI).
22	CLKIN	Master Clock Signal for the device (6 MHz or 7 MHz). Sets the conversion and calibration times.
23	SCLK	Serial Port Clock. Logic input/output. The SCLK pin is configured as an input or output, dependent on the type of serial data transmission (self-clocking or external-clocking) that has been selected by the SM1 and SM2 pins. The SCLK idles high or low depending on the state of the POLARITY pin.
24	$\overline{\text{SYNC}}$	This pin can be an input level triggered active low (similar to a chip select in one case and to a frame sync in the other) or an output (similar to a frame sync) pin depending on SM1, SM2 (see Table XI).

AD7851 ON-CHIP REGISTERS

The AD7851 powers up with a set of default conditions, and the user need not ever write to the device. In this case the AD7851 will operate as a Read-Only ADC. The AD7851 still retains the flexibility for performing a full power-down, and a full self-calibration. Note that the DIN pin should be tied to DGND for operating the AD7851 as a Read-Only ADC.

Extra features and flexibility such as performing different power-down options, different types of calibrations including system calibration, and software conversion start can be selected by writing to the part.

The AD7851 contains a **Control register**, **ADC output data register**, **Status register**, **Test register** and **10 Calibration registers**. The control register is write-only, the ADC output data register and the status register are read-only, and the test and calibration registers are both read/write registers. The test register is used for testing the part and should not be written to.

Addressing the On-Chip Registers

Writing

A write operation to the AD7851 consists of 16 bits. The two MSBs, ADDR0 and ADDR1, are decoded to determine which register is addressed, and the subsequent 14 bits of data are written to the addressed register. It is not until all 16 bits are written that the data is latched into the addressed register. Table I shows the decoding of the address bits, while Figure 4 shows the overall write register hierarchy.

Table I. Write Register Addressing

ADDR1	ADDR0	Comment
0	0	This combination does not address any register so the subsequent 14 data bits are ignored.
0	1	This combination addresses the **TEST REGISTER**. The subsequent 14 data bits are written to the test register.
1	0	This combination addresses the **CALIBRATION REGISTERS**. The subsequent 14 data bits are written to the selected calibration register.
1	1	This combination addresses the **CONTROL REGISTER**. The subsequent 14 data bits are written to the control register.

Reading

To read from the various registers the user must first write to Bits 6 and 7 in the Control Register, RDSLT0 and RDSLT1. These bits are decoded to determine which register is addressed during a read operation. Table II shows the decoding of the read address bits while Figure 5 shows the overall read register hierarchy. The power-up status of these bits is 00 so that the default read will be from the ADC output data register.

Once the read selection bits are set in the control register all subsequent read operations that follow will be from the selected register until the read selection bits are changed in the control register.

Table II. Read Register Addressing

RDSLT1	RDSLT0	Comment
0	0	All successive read operations will be from **ADC OUTPUT DATA REGISTER**. This is the power-up default setting. There will always be four leading zeros when reading from the ADC output data register.
0	1	All successive read operations will be from **TEST REGISTER**.
1	0	All successive read operations will be from **CALIBRATION REGISTERS**.
1	1	All successive read operations will be from **STATUS REGISTER**.

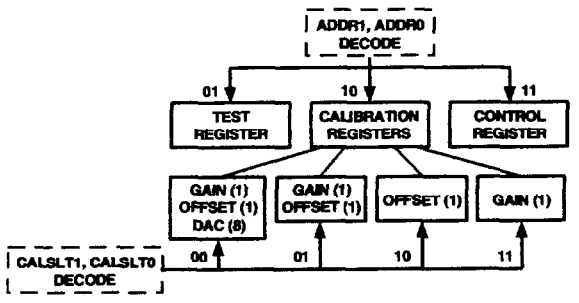


Figure 4. Write Register Hierarchy/Address Decoding

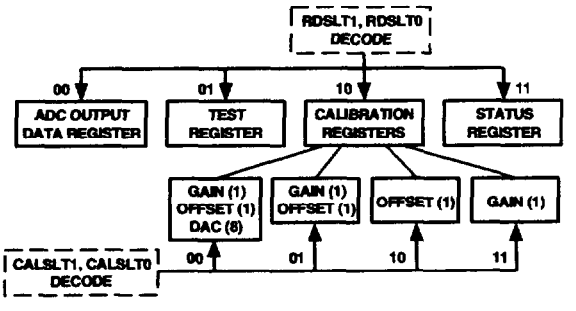


Figure 5. Read Register Hierarchy/Address Decoding

AD7851

CONTROL REGISTER

The arrangement of the control register is shown below. The control register is a write only register and contains 14 bits of data. The control register is selected by putting two 1s in ADDR1 and ADDR0. The function of the bits in the control register are described below. The power-up status of all bits is 0.

MSB

ZERO	ZERO	ZERO	ZERO	PMGT1	PMGT0	RDSLT1

RDSLT0	2/$\overline{3}$ MODE	CONVST	CALMD	CALST1	CALSLT0	STCAL

LSB

Control Register Bit Function Description

Bit	Mnemonic	Comment
13 12 11 10	ZERO ZERO ZERO ZERO	These four bits must be set to 0 when writing to the control register.
9 8	PMGT1 PMGT0	Power Management Bits. These two bits are used with the $\overline{\text{SLEEP}}$ pin for putting the part into various power-down modes (see Power-Down section for more details).
7 6	RDSLT1 RDSLT0	Theses two bits determine which register is addressed for the read operations. See Table II.
5	2/$\overline{3}$ MODE	Interface Mode Select Bit. With this bit set to 0, Interface Mode 2 is enabled. With this bit set to 1, Interface Mode 1 is enabled where DIN is used as an output as well as an input. This bit is set to 0 by default after every read cycle; thus when using Interface Mode 1, this bit needs to be set to 1 in every write cycle.
4	CONVST	Conversion Start Bit. A logic one in this bit position starts a single conversion, and this bit is automatically reset to 0 at the end of conversion. This bit may also used in conjunction with system calibration (see Calibration section on page 21).
3	CALMD	Calibration Mode Bit. A 0 here selects self-calibration and a 1 selects a system calibration (see Table III).
2 1 0	CALSLT1 CALSLT0 STCAL	Calibration Selection Bits and Start Calibration Bit. These bits have two functions. With the STCAL bit set to 1, the CALSLT1 and CALSLT0 bits determine the type of calibration performed by the part (see Table III). The STCAL bit is automatically reset to 0 at the end of calibration. With the STCAL bit set to 0, the CALSLT1 and CALSLT0 bits are decoded to address the calibration register for read/write of calibration coefficients (see section on the calibration registers for more details).

Table III. Calibration Selection

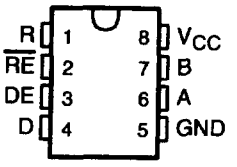
CALMD	CALSLT1	CALSLT0	Calibration Type
0	0	0	A **full internal calibration** is initiated where the internal DAC is calibrated followed by the internal gain error and finally the internal offset error is calibrated out. This is the default setting.
0	0	1	Here the **internal gain error** is calibrated out followed by the **internal offset error** calibrated out.
0	1	0	This calibrates out the **internal offset error** only.
0	1	1	This calibrates out the **internal gain error** only.
1	0	0	A **full system calibration** is initiated here where first the internal DAC is calibrated, followed by the system gain error, and finally the system offset error is calibrated out.
1	0	1	Here the **system gain error** is calibrated out followed by the **system offset error**.
1	1	0	This calibrates out the **system offset error** only.
1	1	1	This calibrates out the **system gain error** only.

SN65176B, SN75176B
DIFFERENTIAL BUS TRANSCEIVERS

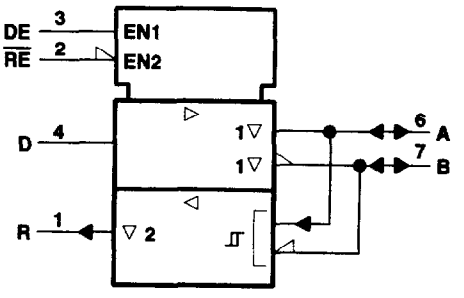
SLLS101A – JULY 1985 – REVISED MAY 1995

- **Bidirectional Transceivers**
- **Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ±60 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operate From Single 5-V Supply**

D OR P PACKAGE
(TOP VIEW)



logic symbol†

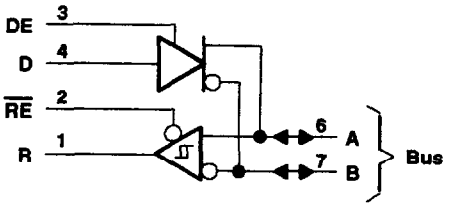


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.11 and X.27.

logic diagram (positive logic)



The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

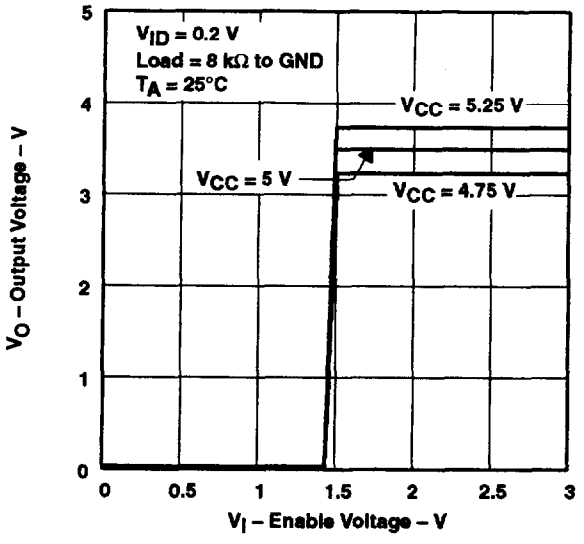


Figure 15

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

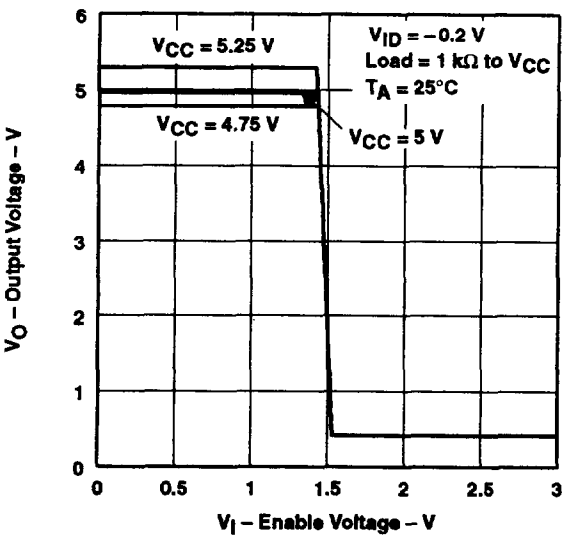


Figure 16

APPLICATION INFORMATION

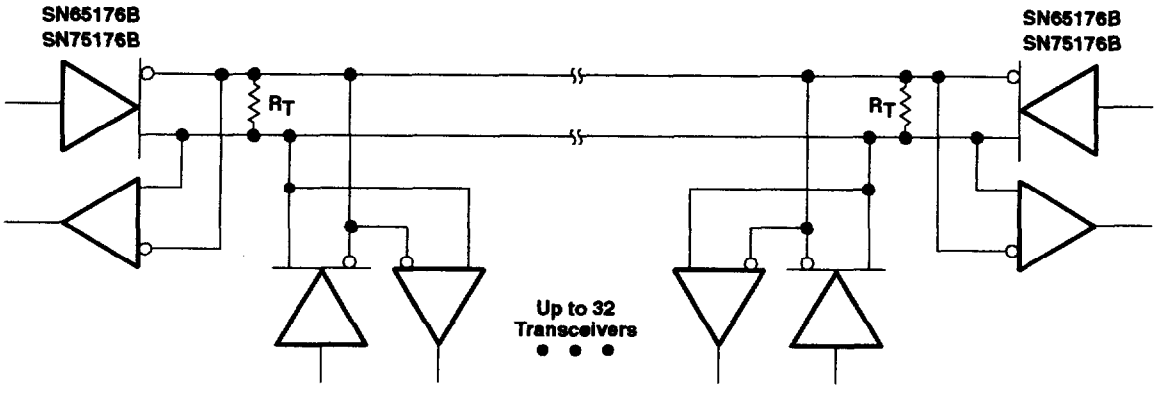


Figure 17. Typical Application Circuit

NOTE: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$)

4 Schéma connexion des balances