B.T.S. ÉLECTRONIQUE

SESSION 2002

ETUDE D'UN SYSTEME TECHNIQUE

SYSTEME DE QUADRIVISION

EXTRAITS DE DOCUMENTS TECHNIQUES

Ce dossier comporte 20 pages

National Semiconductor

October 1989

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD}=5V$, $V_{SS}=0V$ and $V_{EE}=-5V$, analog signals from −5V to +5V can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

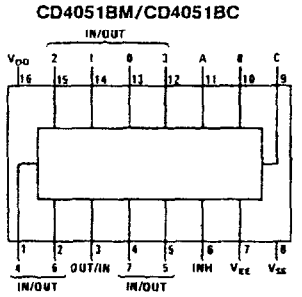
Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD}-V_{EE}=15V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at $V_{DD}-V_{EE}=10V$
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD}-V_{SS}=3-15V$) to switch analog signals to 15 V_{p-p} ($V_{DD}-V_{EE}=15V$)
- Matched switch characteristics: $\Delta R_{ON}=5\Omega$ (typ.) for $V_{DD}-V_{EE}=15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V$
- Binary address decoding on chip

Connection Diagrams

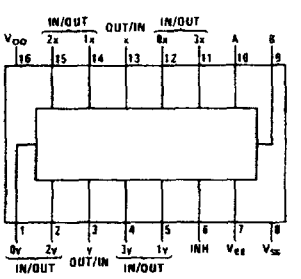
Dual-In-Line Packages

CD4051BM/CD4051BC



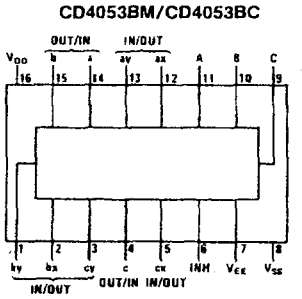
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW

TL/F/5662–1

Order Number CD4051B, CD4052B, or CD4053B

 TL/F/5662

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD}+0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temp. (T_L) (soldering, 10 sec.)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	$+5\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	0V to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
4051BM/4052BM/4053BM	$-55°C$ to $+125°C$
4051BC/4052BC/4053BC	$-40°C$ to $+85°C$

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		−55°C		+25°			+125°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			5			5		150	μA
		$V_{DD}=10V$			10			10		300	μA
		$V_{DD}=15V$			20			20		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE}\le V_{IS}\le V_{DD}$)	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		800		270	1050		1300	Ω
			$V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		310		120	400		550	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		200		80	240		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, $V_{EE}=-7.5V$ $O/I=\pm7.5V$, $I/O=0V$			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V $V_{DD}=7.5V$, $V_{EE}=-7.5V$, $O/I=0V$, $I/O=\pm7.5V$	CD4051		±200		±0.08	±200		±2000	nA
			CD4052		±200		±0.04	±200		±2000	nA
			CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF channels $V_{IS}=V_{DD}$ thru 1 kΩ									
		$V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

CA3306, CA3306A, CA3306C

6-Bit, 15 MSPS, Flash A/D Converters

August 1997

Features

- CMOS Low Power with Video Speed (Typ) 70mW
- Parallel Conversion Technique
- Signal Power Supply Voltage . . . . . 3V to 7.5V
- 15MHz Sampling Rate with Single 5V Supply
- 6-Bit Latched Three-State Output with Overflow Bit
- Pin-for-Pin Retrofit for the CA3300

Applications

- TV Video Digitizing
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- High Speed Oscilloscope Storage/Display
- General Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision

Description

The CA3306 family are CMOS parallel (FLASH) analog-to-digital converters designed for applications demanding both low power consumption and high speed digitization. Digitizing at 15MHz, for example, requires only about 50mW.

The CA3306 family operates over a wide, full scale signal input voltage range of 1V up to the supply voltage. Power consumption is as low as 15mW, depending upon the clock frequency selected. The CA3306 types may be directly retrofitted into CA3300 sockets, offering improved linearity at a lower reference voltage and high operating speed with a 5V supply.

The intrinsic high conversion rate makes the CA3306 types ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3306s in series to increase the resolution of the conversion system. A series connection of two CA3306s may be used to produce a 7-bit high speed converter. Operation of two CA3306s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15MHz to 30MHz).

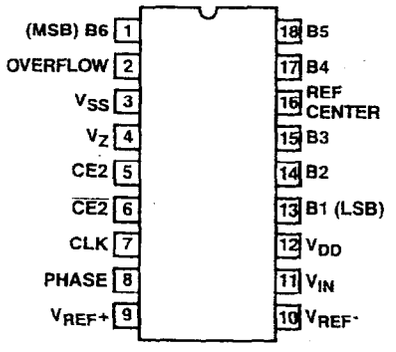
Sixty-four paralleled auto balanced comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the CA3306. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

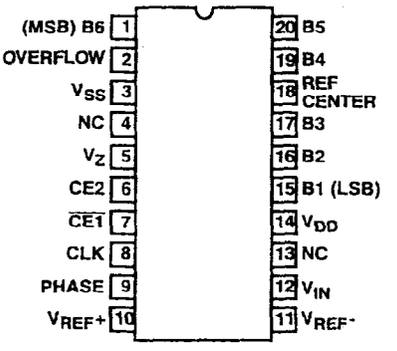
PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3306E	±0.5 LSB	15MHz (67ns)	-40 to 85	18 Ld PDIP	E18.3
CA3306CE	±0.5 LSB	10MHz (100ns)	-40 to 85	18 Ld PDIP	E18.3
CA3306M	±0.5 LSB	15MHz (67ns)	-40 to 85	20 Ld SOIC	M20.3
CA3306CM	±0.5 LSB	10MHz (100ns)	-40 to 85	20 Ld SOIC	M20.3
CA3306D	±0.5 LSB	15MHz (67ns)	-55 to 125	18 Ld SBDIP	D18.3
CA3306CD	±0.5 LSB	10MHz (100ns)	-55 to 125	18 Ld SBDIP	D18.3
CA3306J3	±0.5 LSB	15MHz (67ns)	-55 to 125	20 Ld CLCC	J20.B
CA3306J3	±0.5 LSB	10MHz (100ns)	-55 to 125	20 Ld CLCC	J20.B

Pinouts

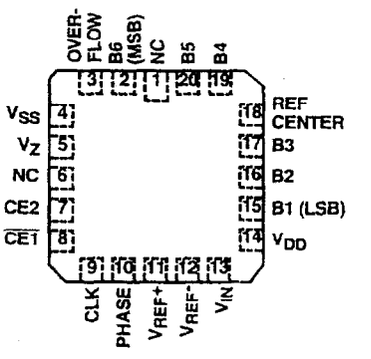
CA3306 (PDIP, SBDIP)
TOP VIEW



CA3306 (SOIC)
TOP VIEW



CA3306 (CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number 3102.1

TABLE 1. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	B1 - B6	OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't care

TABLE 2. OUTPUT CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE V_{REF} 6.40 (V)	V_{REF} 5.12 (V)	V_{REF} 4.80 (V)	V_{REF} 3.20 (V)	BINARY OUTPUT CODE (LSB) OF	B6	B5	B4	B3	B2	B1	DECIMAL COUNT
Zero	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.10	0.08	0.075	0.05	0	0	0	0	0	0	1	1
2 LSB	0.20	0.16	0.15	0.10	0	0	0	0	0	1	0	2
•		•						•				•
•		•						•				•
•		•						•				•
•		•						•				•
$^1/_2$ Full Scale - 1 LSB	3.10	2.48	2.325	1.55	0	0	1	1	1	1	1	31
$^1/_2$ Full Scale	3.20	2.56	2.40	1.60	0	1	0	0	0	0	0	32
$^1/_2$ Full Scale + 1 LSB	3.30	2.64	2.475	1.65	0	1	0	0	0	0	1	33
•		•						•				•
•		•						•				•
•		•						•				•
•		•						•				•
Full Scale - 1 LSB	6.20	4.96	4.65	3.10	0	1	1	1	1	1	0	62
Full Scale	6.30	5.04	4.725	3.15	0	1	1	1	1	1	1	63
Overflow	6.40	5.12	4.80	3.20	1	1	1	1	1	1	1	127

NOTE:

1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

SN5474, SN54LS74A, SN54S74
SN7474, SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

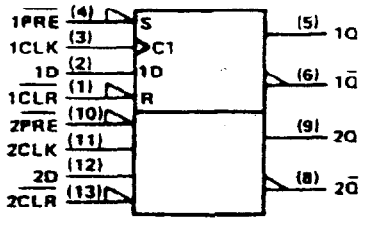
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

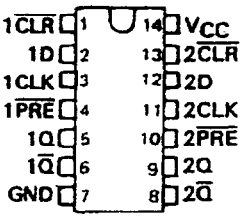
logic symbol‡



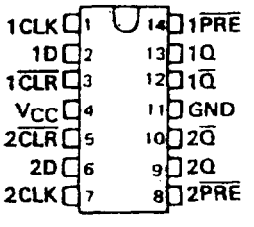
‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

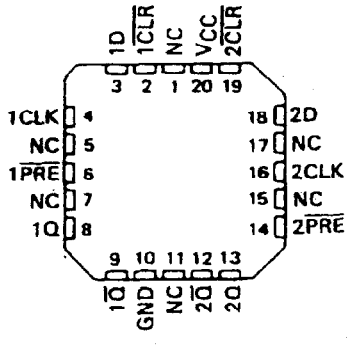
SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

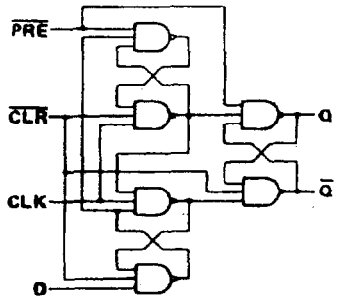


SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS155A

CD54/74HC164, CD54/74HCT164

High Speed CMOS Logic 8-Bit Serial-In/Parallel-Out Shift Register

October 1997 - Revised May 2000

Features

- Buffered Inputs
- Asynchronous Master Reset
- Typical f_{MAX} = 50MHz at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The 'HC164 and 'HCT164 are 8-bit serial-in parallel-out shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CP). A LOW on the Master Reset ($\overline{MR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided, either one can be used as a Data Enable control.

Ordering Information

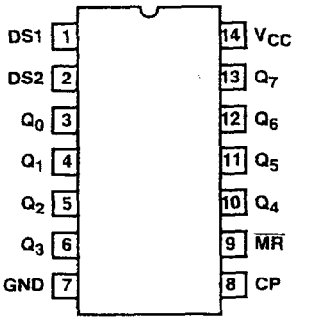
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC164F	-55 to 125	14 Ld CERDIP
CD54HC164F3A	-55 to 125	14 Ld CERDIP
CD74HC164E	-55 to 125	14 Ld PDIP
CD74HC164M	-55 to 125	14 Ld SOIC
CD54HCT164F3A	-55 to 125	14 Ld CERDIP
CD74HCT164E	-55 to 125	14 Ld PDIP
CD74HCT164M	-55 to 125	14 Ld SOIC

NOTE:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

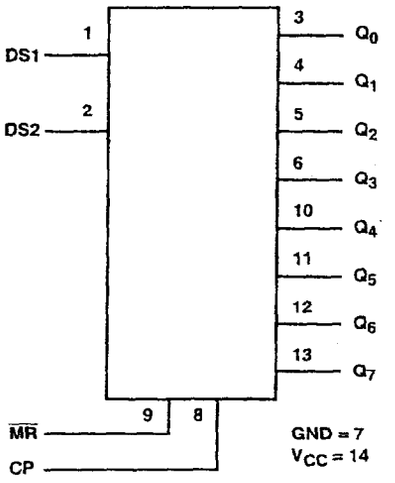
Pinout

CD54HC164, CD54HCT164
(CERDIP)
CD74HC164, CD74HCT164
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



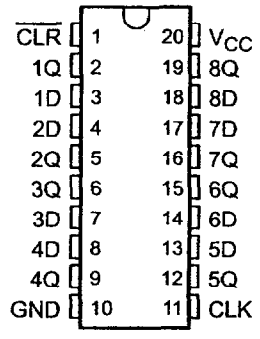
TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1	DS2	Q_0	$Q_1 - Q_7$
RESET (CLEAR)	L	X	X	X	L	L - L
Shift	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

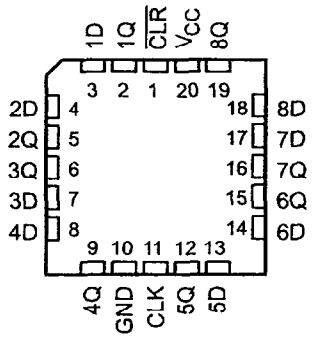
NOTES:
H = High Voltage Level.
h = High Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition.
l = Low Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition.
L = Low Voltage Level.
X = Don't Care.
↑ = Transition from Low to High Level.
q_n = Lower Case Letters Indicate The State Of the Reference Input Clock Transition.

- **Inputs Are TTL-Voltage Compatible**
- **Contain Eight D-Type Flip-Flops**
- **Direct Clear Input**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT273 . . . J OR W PACKAGE
SN74HCT273 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT273 . . . FK PACKAGE
(TOP VIEW)



description

These devices are positive-edge-triggered D-type flip-flops with a common enable input. The 'HCT273 are similar to the 'HCT377, but feature a common clear enable ($\overline{CLR}$) input instead of a latched clock.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. The circuits are designed to prevent false clocking by transitions at $\overline{CLR}$.

The SN54HCT273 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT273 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

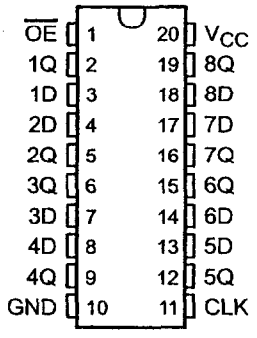
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

SN54HCT374, SN74HCT374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

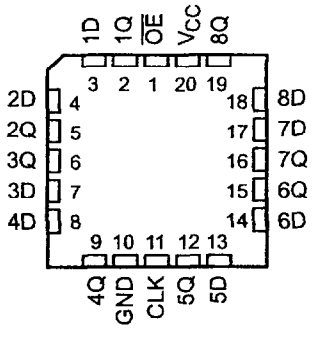
SCLS005A – MARCH 1984 – REVISED JANUARY 1996

- **Inputs Are TTL-Voltage Compatible**
- **Eight D-Type Flip-Flops in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HCT374 . . . J OR W PACKAGE
SN74HCT374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT374 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'HCT374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HCT374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

NEC Electronics Inc.

μPD41464
65,536 x 4-Bit
Dynamic NMOS RAM

Description

The μPD41464 is a 65,536-word by 4-bit dynamic RAM designed to operate from a single + 5-volt power supply and fabricated with a double polylayer, N-channel silicon-gate process for high density, high performance, and high reliability. A single-transistor storage cell and advanced dynamic circuitry ensure minimum power dissipation, while an on-chip feature internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or hidden refresh cycle, data is held by holding $\overline{CAS}$ low. Data input and output is returned to high impedance by returning $\overline{CAS}$ high. Hidden refreshing allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address, by means of $\overline{RAS}$-only refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms refresh period.

Features

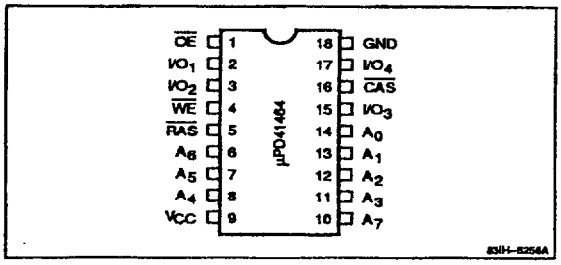
- 65,536-word by 4-bit organization
- Single + 5-volt ±10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Low power dissipation
  - —28 mA max (standby)
  - —440 mW (active, $t_{RC} = t_{RC}$ min)
- Nonlatched, TTL-compatible inputs and outputs
- Low input capacitance
- 256 refresh cycles every 4 ms
- Standard 18-pin plastic DIP and PLCC packaging

Ordering Information

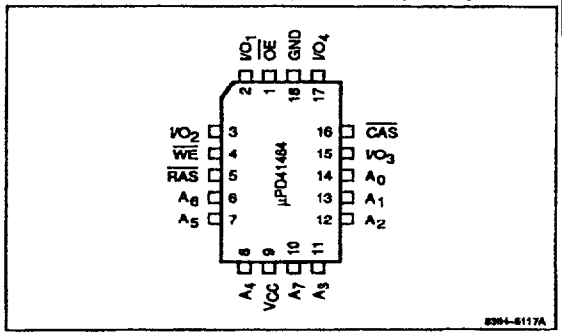
Part Number	Row Access Time (max)	Package
μPD41464C-80	80 ns	18-pin plastic DIP
C-10	100 ns	
C-12	120 ns	
μPD41464L-80	80 ns	18-pin PLCC
L-10	100 ns	
L-12	120 ns	

Pin Configurations

18-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



3b

Pin Identification

Name	Function
A_0 - A_7	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	A_0 through A_7
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 through I/O_4

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1	V
Input voltage, low	V_{IL}	−1		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Block Diagram