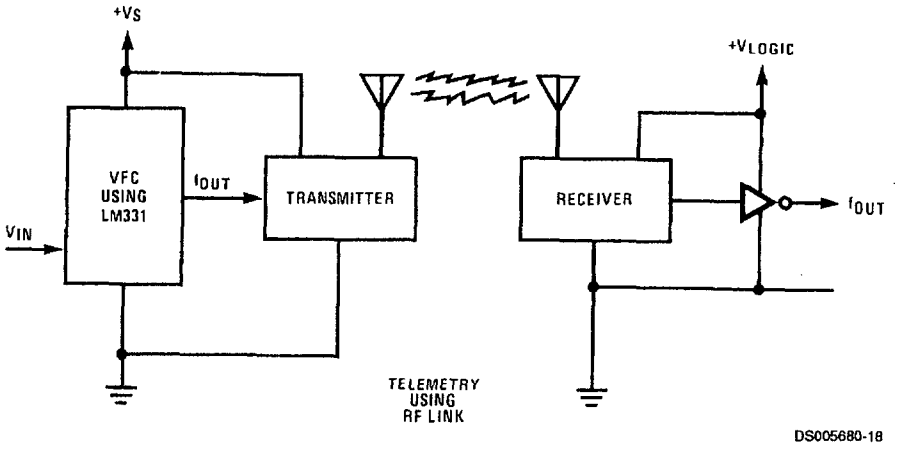
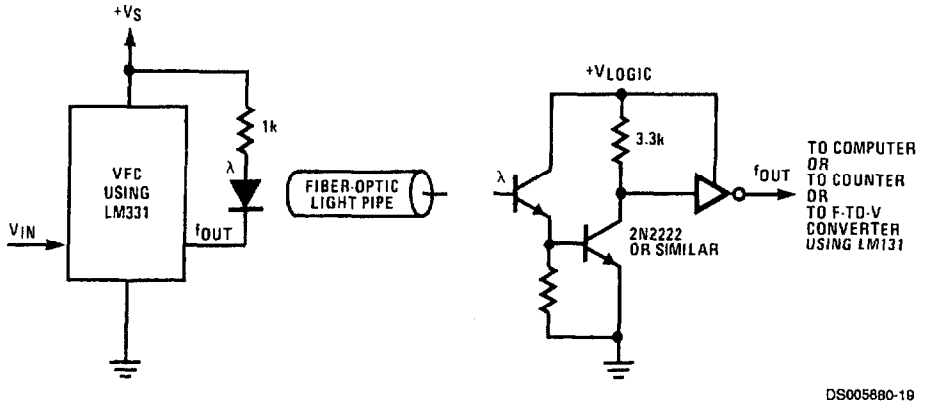
## Typical Applications (Continued)

**Voltage-to-Frequency Converter with Isolators**




DS005680-18

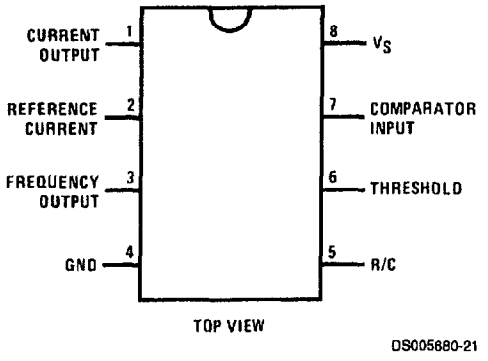
**Voltage-to-Frequency Converter with Isolators**




DS005680-19

## Connection Diagram

**Dual-In-Line Package**




DS005680-21

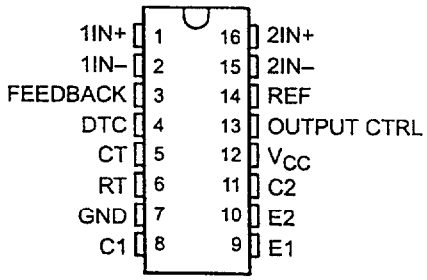
**Order Number LM231AN, LM231N, LM331AN, *or* LM331N**
**See NS Package Number N08E**

# TL494
# PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS074D – JANUARY 1983 – REVISED MAY 2002

- Complete PWM Power-Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source Current
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance
- Circuit Architecture Allows Easy Synchronization

D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)




## description

The TL494 incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the flexibility to tailor the power-supply control circuitry to a specific application.

The TL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from –0.3 V to $V_{CC}$ – 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 provides for push-pull or single-ended output operation, which can be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494C is characterized for operation from 0°C to 70°C. The TL494I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

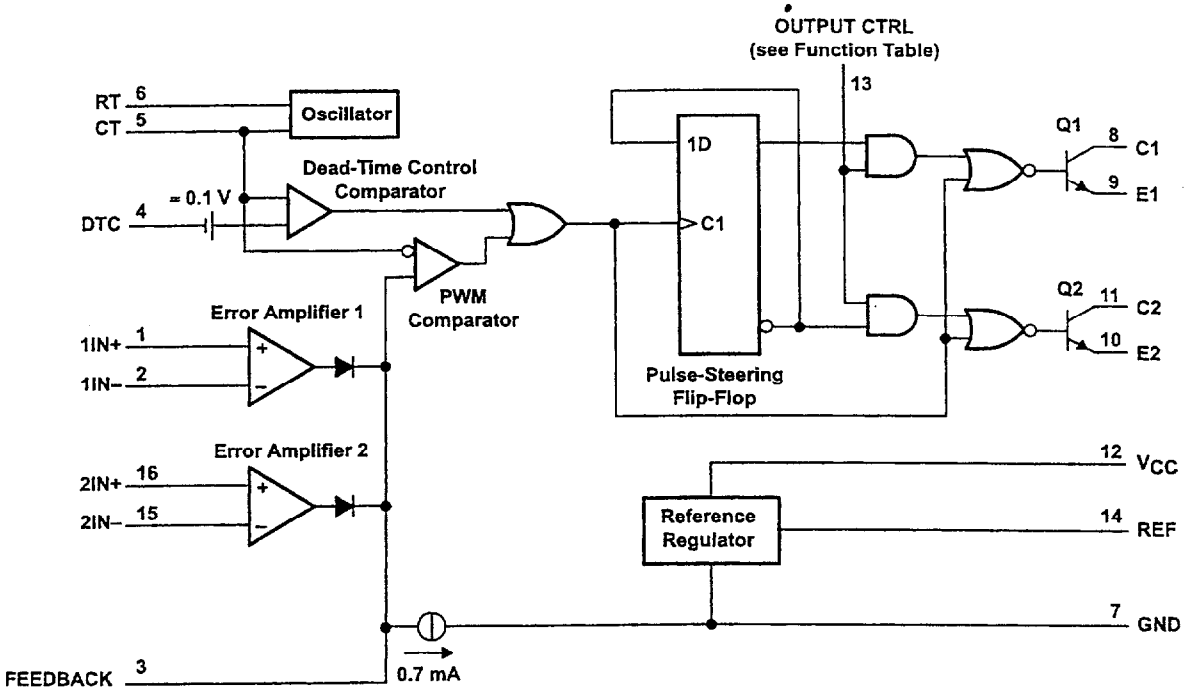
| $T_A$ | PACKAGED DEVICES | | | | |
|---|---|---|---|---|---|
| | SMALL OUTLINE (D) | PLASTIC DIP (N) | SMALL OUTLINE (NS) | SHRINK SMALL OUTLINE (DB) | THIN SHRINK SMALL OUTLINE (PW) |
| 0°C to 70°C | TL494CD | TL494CN | TL494CNS | TL494CDB | TL494CPW |
| –40°C to 85°C | TL494ID | TL494IN | — | — | — |

The D, DB, NS, and PW packages are available taped and reeled. Add the suffix R to device type (e.g., TL494CDR).

FUNCTION TABLE

| INPUT TO OUTPUT CTRL | OUTPUT FUNCTION |
|---|---|
| $V_I$ = GND | Single-ended or parallel output |
| $V_I = V_{ref}$ | Normal push-pull operation |

## functional block diagram



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 41 V
Amplifier input voltage, $V_I$ . . . . . $V_{CC}$ + 0.3 V
Collector output voltage, $V_O$ . . . . . 41 V
Collector output current, $I_O$ . . . . . 250 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2 and 3): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
PW package . . . . . 108°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 7 | 40 | V |
| $V_I$ | Amplifier input voltage | | –0.3 | $V_{CC}$–2 | V |
| $V_O$ | Collector output voltage | | | 40 | V |
| | Collector output current (each transistor) | | | 200 | mA |
| | Current into feedback terminal | | | 0.3 | mA |
| $f_{osc}$ | Oscillator frequency | | 1 | 300 | kHz |
| $C_T$ | Timing capacitor | | 0.47 | 10000 | nF |
| $R_T$ | Timing resistor | | 1.8 | 500 | kΩ |
| $T_A$ | Operating free-air temperature | TL494C | 0 | 70 | °C |
| | | TL494I | –40 | 85 | |

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 15 V, f = 10 kHz (unless otherwise noted)

### reference section

| PARAMETER | TEST CONDITIONS† | TL494C, TL494I | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP‡ | MAX | |
| Output voltage (REF) | $I_O$ = 1 mA | 4.75 | 5 | 5.25 | V |
| Input regulation | $V_{CC}$ = 7 V to 40 V | | 2 | 25 | mV |
| Output regulation | $I_O$ = 1 mA to 10 mA | | 1 | 15 | mV |
| Output voltage change with temperature | $\Delta T_A$ = MIN to MAX | | 2 | 10 | mV/V |
| Short-circuit output current§ | REF = 0 V | | 25 | | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for parameter changes with temperature, are at $T_A$ = 25°C.
§ Duration of the short circuit should not exceed one second.

### oscillator section, $C_T$ = 0.01 µF, $R_T$ = 12 kΩ (see Figure 1)

| PARAMETER | TEST CONDITIONS† | TL494, TL494I | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP‡ | MAX | |
| Frequency | | | 10 | | kHz |
| Standard deviation of frequency¶ | All values of $V_{CC}$, CT, RT, and $T_A$ constant | | 100 | | Hz/kHz |
| Frequency change with voltage | $V_{CC}$ = 7 V to 40 V, $T_A$ = 25°C | | 1 | | Hz/kHz |
| Frequency change with temperature# | $\Delta T_A$ = MIN to MAX | | | 10 | Hz/kHz |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except for parameter changes with temperature, are at $T_A$ = 25°C.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N-1}}$$

# Temperature coefficient of timing capacitor and timing resistor are not taken into account.

### error-amplifier section (see Figure 2)

| PARAMETER | TEST CONDITIONS | TL494, TL494I | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP‡ | MAX | |
| Input offset voltage | $V_O$ (FEEDBACK) = 2.5 V | | 2 | 10 | mV |
| Input offset current | $V_O$ (FEEDBACK) = 2.5 V | | 25 | 250 | nA |
| Input bias current | $V_O$ (FEEDBACK) = 2.5 V | | 0.2 | 1 | µA |
| Common-mode input voltage range | $V_{CC}$ = 7 V to 40 V | –0.3 to $V_{CC}$–2 | | | V |
| Open-loop voltage amplification | $\Delta V_O$ = 3 V, $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 3.5 V | 70 | 95 | | dB |
| Unity-gain bandwidth | $V_O$ = 0.5 V to 3.5 V, $R_L$ = 2 kΩ | | 800 | | kHz |
| Common-mode rejection ratio | $\Delta V_O$ = 40 V, $T_A$ = 25°C | 65 | 80 | | dB |
| Output sink current (FEEDBACK) | $V_{ID}$ = –15 mV to –5 V, V (FEEDBACK) = 0.7 V | 0.3 | 0.7 | | mA |
| Output source current (FEEDBACK) | $V_{ID}$ = 15 mV to 5 V, V (FEEDBACK) = 3.5 V | –2 | | | mA |

‡ All typical values, except for parameter changes with temperature, are at $T_A$ = 25°C.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 15 V, f = 10 kHz (unless otherwise noted)

### output section

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Collector off-state current | | $V_{CE}$ = 40 V, | $V_{CC}$ = 40 V | | 2 | 100 | μA |
| Emitter off-state current | | $V_{CC}$ = $V_C$ = 40 V, | $V_E$ = 0 | | | −100 | μA |
| Collector-emitter saturation voltage | Common emitter | $V_E$ = 0, | $I_C$ = 200 mA | | 1.1 | 1.3 | V |
| | Emitter follower | $V_{O(C1 \text{ or } C2)}$ = 15 V, | $I_E$ = −200 mA | | 1.5 | 2.5 | |
| Output control input current | | $V_I$ = $V_{ref}$ | | | | 3.5 | mA |

† All typical values except for temperature coefficient are at $T_A$ = 25°C.

### dead-time control section (see Figure 1)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|
| Input bias current (DEAD-TIME CTRL) | $V_I$ = 0 to 5.25 V | | −2 | −10 | μA |
| Maximum duty cycle, each output | $V_I$ (DEAD-TIME CTRL) = 0, $C_T$ = 0.01 μF, $R_T$ = 12 kΩ | | 45% | | |
| Input threshold voltage (DEAD-TIME CTRL) | Zero duty cycle | | 3 | 3.3 | V |
| | Maximum duty cycle | 0 | | | |

† All typical values except for temperature coefficient are at $T_A$ = 25°C.

### PWM comparator section (see Figure 1)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|
| Input threshold voltage (FEEDBACK) | Zero duty cycle | | 4 | 4.5 | V |
| Input sink current (FEEDBACK) | V (FEEDBACK) = 0.7 V | 0.3 | 0.7 | | mA |

† All typical values except for temperature coefficient are at $T_A$ = 25°C.

### total device

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| Standby supply current | RT = $V_{ref}$, All other inputs and outputs open | $V_{CC}$ = 15 V | | 6 | 10 | mA |
| | | $V_{CC}$ = 40 V | | 9 | 15 | |
| Average supply current | $V_I$ (DEAD-TIME CTRL) = 2 V, | See Figure 1 | | 7.5 | | mA |

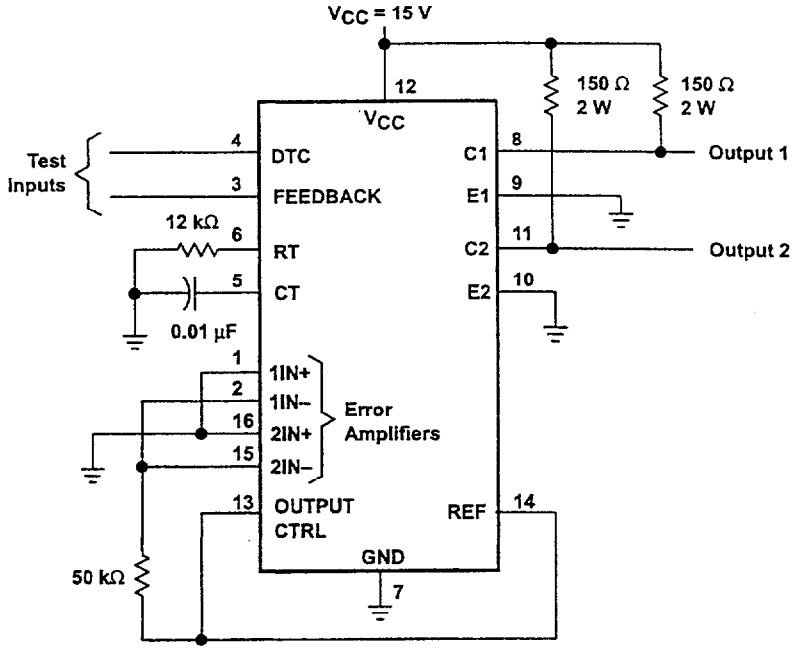
† All typical values except for temperature coefficient are at $T_A$ = 25°C.

## switching characteristics, $T_A$ = 25°C

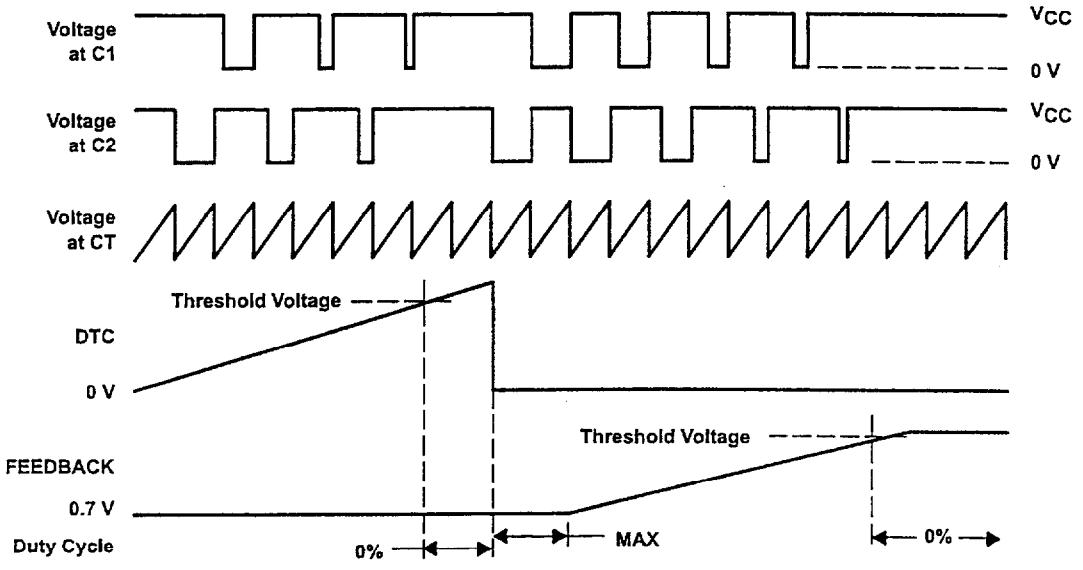
| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| Rise time | Common-emitter configuration, | See Figure 3 | | 100 | 200 | ns |
| Fall time | | | | 25 | 100 | ns |
| Rise time | Emitter-follower configuration, | See Figure 4 | | 100 | 200 | ns |
| Fall time | | | | 40 | 100 | ns |

† All typical values except for temperature coefficient are at $T_A$ = 25°C.

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

**Figure 1. Operational Test Circuit and Waveforms**

## PARAMETER MEASUREMENT INFORMATION

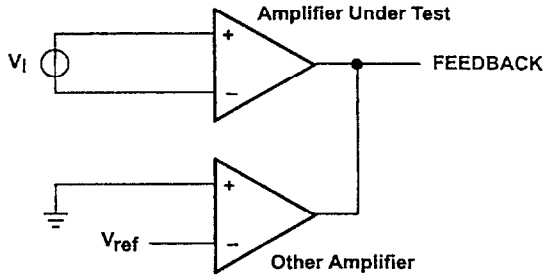
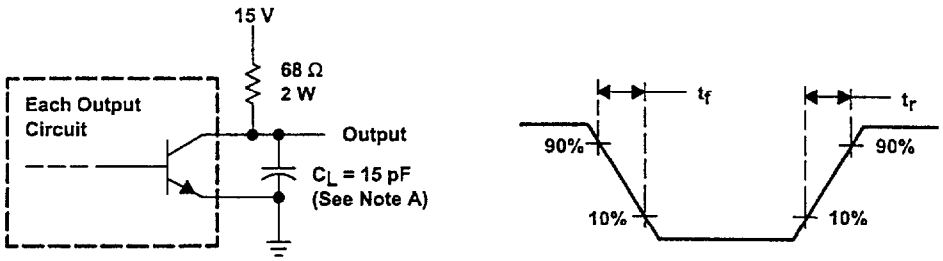



Figure 2. Amplifier Characteristics

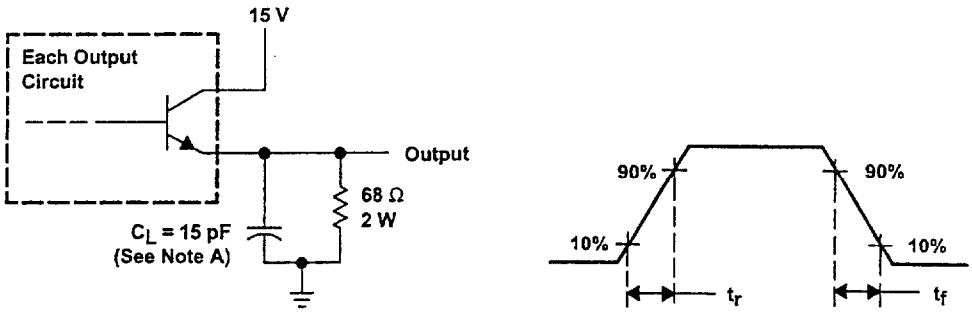



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

NOTE A: $C_L$ includes probe and jig capacitance.

Figure 3. Common-Emitter Configuration




TEST CIRCUIT

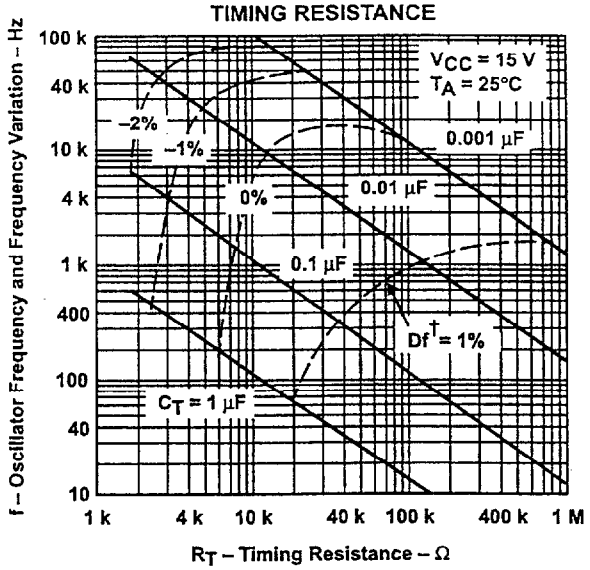
OUTPUT VOLTAGE WAVEFORM

NOTE A: $C_L$ includes probe and jig capacitance.

Figure 4. Emitter-Follower Configuration

## TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† vs TIMING RESISTANCE




† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 5

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

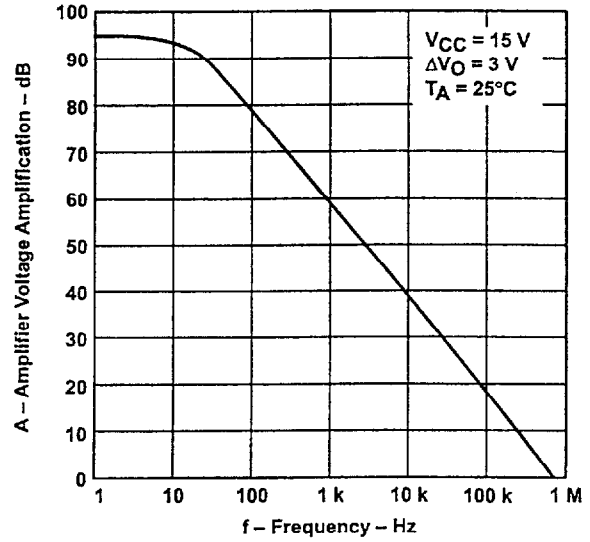


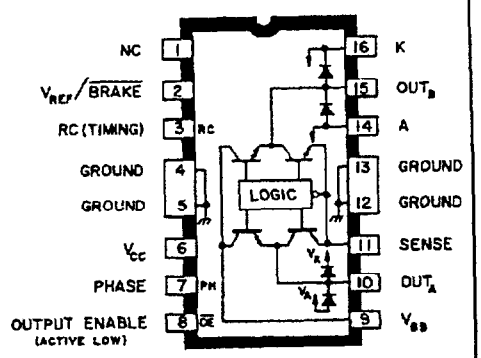

Figure 6

# 2953 AND 2954

Data Sheet 29319.2B

## FULL-BRIDGE PWM MOTOR DRIVERS

### UDN2953B




Dwg. No. A-13,024

The UDN2953B and UDN2954W are designed for bidirectional control of dc or stepper motors with continuous output currents to 2 A and peak start-up currents as high as 3.5 A. For pulse-width modulated (chopped-mode) operation, the output current is determined by the user's selection of a reference voltage and sensing resistor while the OFF pulse duration is set by an external RC timing network. PWM operation is characterized by maximum efficiency and low power-dissipation levels. Extensive internal circuit protection includes thermal shutdown with hysteresis, transient-suppression diodes, and crossover current protection.

When the $V_{REF}$/$\overline{BRAKE}$ pin is low (<0.8 V), the braking function is enabled. This turns both sink drivers OFF and the source drivers are turned ON. When $V_{REF}$/$\overline{BRAKE}$ is set above 2.4 V, that voltage (and the current sensing resistor) determines the load current trip point. An RC TIMING pin is available to use for an internal one-shot to control load current decay time.

The UDN2953B driver is supplied in a 16-pin dual-in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. The UDN2954W, for higher package power dissipation requirements, is supplied in a 12-pin single in-line power tab package. In both package styles, the heat sink is at ground potential and needs no insulation.

## FEATURES

- 50 V Output Voltage Rating
- 2 A Continuous Output Rating
- Internal Flyback Diodes
- Thermal Shutdown
- Crossover Current Protection
- BRAKE, ENABLE, and Current-Limit Functions

### ABSOLUTE MAXIMUM RATINGS at $T_J \le +150°C$

Motor Supply Voltage, $V_{BB}$ ..... 50 V
Output Current, $I_{OUT}$
(Peak) ..... ±3.5 A
(Continuous) ..... ±2.0 A
Flyback Diode Voltage, $V_K$ ..... $V_{BB}$
Minimum Clamp Diode Voltage, $V_A$ ..... Ground
Logic Supply Voltage, $V_{CC}$ ..... 7.0 V
Logic Input Voltage, $V_{PHASE}$, $V_{ENABLE}$ ..... $V_{BB}$
Sense Voltage, $V_{SENSE}$ ..... 1.5 V
Reference Voltage, $V_{REF}$/$\overline{BRAKE}$ ..... 15 V
Package Power Dissipation, $P_D$ ..... See Graphs
Operating Temperature Range, $T_A$ ..... -20°C to +85°C
Storage Temperature Range, $T_S$ ..... -55°C to +150°C

Always order by complete part number:

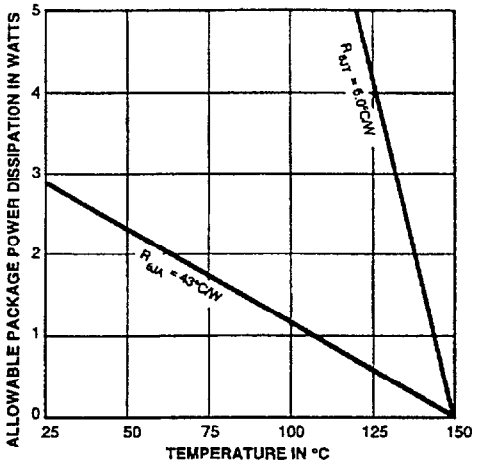
| Part Number | Package |
|---|---|
| UDN2953B | 16-Pin DIP |
| UDN2954W | 12-Pin Power-Tab SIP |



ELEST

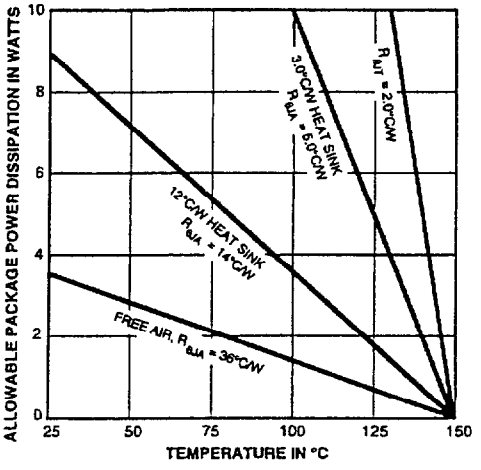
# 2953 AND 2954
## *FULL-BRIDGE PWM MOTOR DRIVERS*

### UDN2953B




Dwg. GP-010B

### UDN2954W



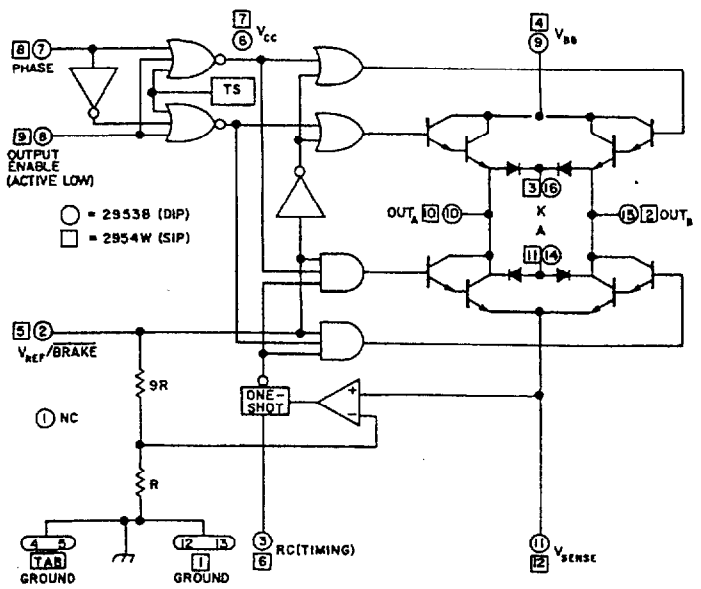

Dwg. GP-012A

### TRUTH TABLE

| Output Enable | Phase | $V_{REF}/\overline{BRAKE}$ | $Out_A$ | $Out_B$ |
|---|---|---|---|---|
| Low | High | > 2.4 V | High | Low |
| Low | Low | > 2.4 V | Low | High |
| High | X | > 2.4 V | Open | Open |
| X | X | < 0.8 V | High | High |

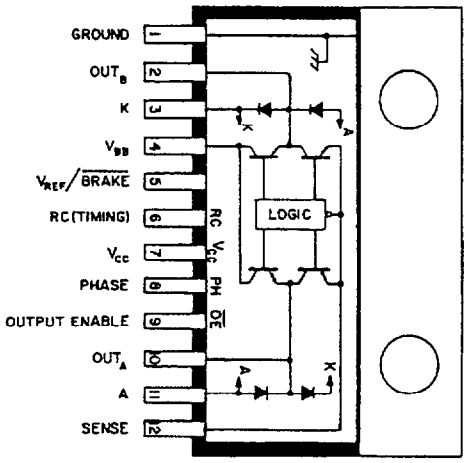
X = Irrelevant

### FUNCTIONAL BLOCK DIAGRAM




Dwg. No. A-13,028

### UDN2954W




Dwg. No. A-13,023


Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000




ELEST

**ELECTRICAL CHARACTERISTICS at $T_A$ = +25°C, $T_J \leq$ +150°C, $V_{BB}$ = 50 V, $V_{CC}$ = 5 V, $V_{SENSE}$ = 0 V, RC = 20 kΩ/470 pF to Ground.**

| Characteristic | Symbol | Test Conditions | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| **Output Drivers ($OUT_A$ or $OUT_B$)** | | | | | | |
| Output Supply Range | $V_{BB}$ | | 6.5 | — | 50 | V |
| Output Leakage Current | $I_{CEX}$ | $V_{ENABLE}$ = 5 V, $V_{OUT}$ = $V_{BB}$, (note) | — | — | 50 | µA |
| | | $V_{ENABLE}$ = 5 V, $V_{OUT}$ = 0 V, (note) | — | — | -50 | µA |
| Output Sustaining Voltage | $V_{CE(sus)}$ | $I_{OUT}$ = ±2 A, L = 2 mH | 50 | — | — | V |
| Output Saturation Voltage | $V_{CE(SAT)}$ | $V_{ENABLE}$ = 0 V, $I_{OUT}$ = ±0.5 A | — | 1.0 | 1.2 | V |
| | | $V_{ENABLE}$ = 0 V, $I_{OUT}$ = ±1.0 A | — | 1.2 | 1.4 | V |
| | | $V_{ENABLE}$ = 0 V, $I_{OUT}$ = ± 2.0 A | — | 1.5 | 1.8 | V |
| Clamp Diode Leakage Current | $I_R$ | $V_R$ = 50 V | — | — | 50 | µA |
| Clamp Diode Forward Voltage | $V_F$ | $I_F$ = 2 A | — | 1.8 | 2.2 | V |
| Motor Supply Current | $I_{BB(ON)}$ | $V_{ENABLE}$ = 0.8 V, $V_{REF}$ = 2.4 V, No Load | — | 20 | 30 | mA |
| | $I_{BB(OFF)}$ | $V_{ENABLE}$ = $V_{REF}$ = 2.4 V, No Load | — | 2.5 | 3.5 | mA |
| | | $V_{ENABLE}$ = 5 V, $V_{REF}$ = 0.8 V, No Load | — | 40 | 60 | mA |
| **Control Logic** | | | | | | |
| Logic Supply Range | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| Logic Input Current | $I_{IN(1)}$ | All Inputs = 2.4 V | — | <-1.0 | -10 | µA |
| | $I_{IN(0)}$ | All Inputs = 0.8 V | — | -50 | -200 | µA |
| Logic Input Voltage | $V_{IN(1)}$ | All Inputs | 2.4 | — | — | V |
| | $V_{IN(0)}$ | All Inputs | — | — | 0.8 | V |
| $V_{REF}$ Open-Circuit Voltage | $V_{REF(OPEN)}$ | $I_{REF}$ = 0 | — | $V_{CC}$/2 | — | V |
| Current Limit Threshold | | $V_{REF}/V_{SENSE}$ at Trip Point | 9.5 | 10 | 10.5 | — |
| Turn-On Delay | $t_{on}$ | All Drivers | — | 1.0 | — | µs |
| Turn-Off Delay | $t_{off}$ | All Drivers | — | 1.0 | — | µs |
| Thermal Shutdown Temp. | $T_J$ | | — | 165 | — | °C |
| Logic Supply Current | $I_{CC}$ | $V_{ENABLE}$ = $V_{REF}$ = 2.4 V | — | 15 | 20 | mA |
| | | $V_{ENABLE}$ = 0.8 V, $V_{REF}$ = 2.4 V | — | 22 | 30 | mA |

NOTE: Tests performed at $OUT_B$ with $V_{PHASE}$ = 0.8 V and at $OUT_A$ with $V_{PHASE}$ = 2.4 V

# 2953 AND 2954
# *FULL-BRIDGE PWM MOTOR DRIVERS*

## APPLICATIONS INFORMATION

The UDN2953B and UDN2954W full-bridge motion control ICs are designed for pulse-width-modulated (PWM ) bidirectional interface to many types of dc (brush) servo, brushless dc, and 2-phase stepper motors. These power ICs permit various techniques of direct motor interface and offer internally and externally programmed current control. Pulse-width-modulated output current can be regulated by an (external) PWM control signal or use of an external sensing resistor ($R_{SENSE}$) in combination with an RC network and/or voltage reference.

The output current trip point or sense resistor formulas are:

$$I_{TRIP} = \frac{V_{REF}}{10\ R_{SENSE}}$$

$$R_{SENSE} = \frac{V_{REF}}{10\ I_{TRIP}}$$

The allowable reference voltage range is from 2.4 V to 15 V. If unconnected, the reference input ($V_{REF}$) defaults to $V_{CC}/2$ (refer to Figure 1) and $I_{TRIP}$ = 0.5 A (per typical application where $R_S$ = 0.5 Ω).

When the motor current attains the specified design value, the internal comparator triggers the monostable ('one-shot') multivibrator, which disables (switches OFF) the sink (lower) output. The actual load current may vary slightly, and the difference is (chiefly) related to the circuit propagation delays between comparator (trip point) command and power output switching. Applications involving very-low inductance windings may necessitate specific consideration; typical circuit delays ($t_d$) are about 2 µs.

After the sink ('low-side') output is switched OFF, motor current starts to decay, and the circulation path is through the ON source (upper) drive output and the flyback diode protecting the sink (lower) output. The output OFF interval is set by an external RC timing network connected to the monostable. The magnitude of the current decay is directly related to the OFF period and the duration should allow the current level to drop below the trip point before reactivating the sink output. This ON-OFF PWM cycle repeats, sustaining the desired average current to the motor winding, and continues free-running until a new input command switches the output state. The RC network values range from 20 kΩ to 100 kΩ for resistors, and capacitor values from 200 pF to 500 pF. The parallel RC network establishes the $t_{off}$ interval and directly affects the decaying motor current.

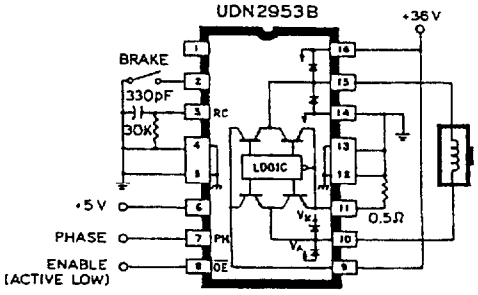
Internal timing circuitry is an alternative to the external RC timing network. However, with internal timing the logic supply current rises approximately 6 mA. Connecting the RC input to the logic supply activates internal circuitry; $t_{off}$ = 12 µs with $V_{CC}$ = +5 V and $T_A$ = +25 C, and increases with temperature.

The sink (lower) output is repeatedly re-enabled until the motor is reversed, braked, or stopped. Current control via pulse modulating the lower outputs is based on the dynamic characteristics of the much faster NPN Darlington outputs.

Another method of controlling motor current involves external circuitry to pulse modulate the OUTPUT ENABLE pin. Switching (toggling) the OUTPUT ENABLE affects both the sink (low-side) and upper (high-side) outputs. Both lower and upper transient-protection diodes conduct during the OFF interval. This method of operation produces very rapid current decay. The sink driver parallel diodes (common anode pin) are connected to ground; the source output flyback diodes (common cathode pin) are connected to the motor supply ($V_{BB}$). The RC input pin is to be terminated to ground through 20 kΩ (minimum).

The motor is braked by simultaneously activating both source driver outputs and disabling both sink outputs. Basically, this shorts both terminals of the motor winding to the supply. The back EMF (electromotive force) of the motor develops current which functions as a dynamic brake. Typically, the braking current approaches the values related to a locked rotor (or stall) condition. Fundamentally, locked rotor (or stall) current is dependent upon the motor winding impedance and driver output ON characteristics. Internal current control circuitry is not operational during braking. Therefore, designers should exercise caution to ensure that the current produced by the back EMF does not exceed the absolute maximum ratings of the power outputs.

## TYPICAL APPLICATION




Dwg. No. A-12,649B

NOTE: Pin 3 must be connected to an RC network as shown, or to $V_{CC}$. It must **NOT** be left unconnected.


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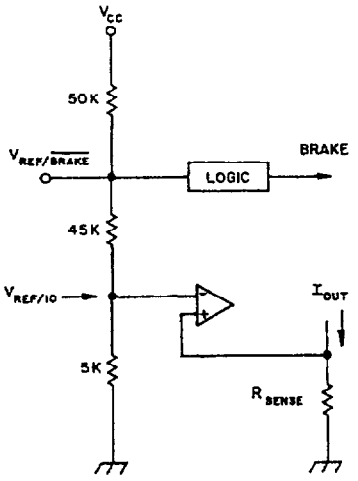
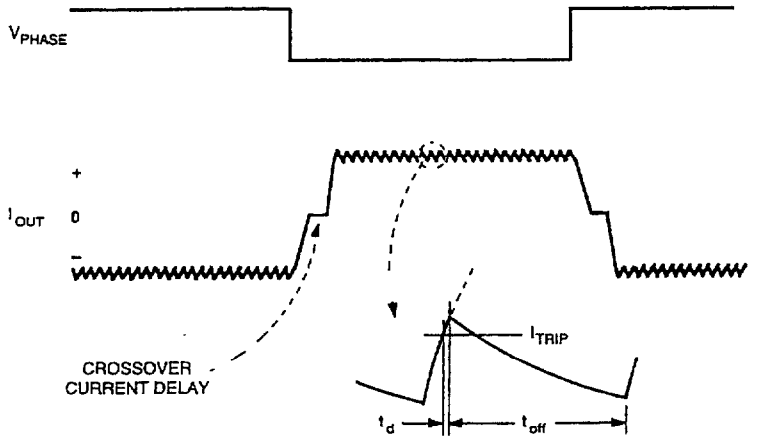
**Figure 1**




Dwg. No. A-13,025

**Figure 2**




Dwg. WM-003-1

In bidirectional drive applications, especially dc (brush) servos, the PHASE input is utilized for direction control. The current generated by back EMF at reversal is comparable to that of dynamic braking, and should be limited to the absolute maximum output current rating.

An internally generated deadtime (approximately 3 µs) precludes the high crossover (or 'shoot-through') currents associated with momentary, overlapping conduction of both upper and lower outputs. This very abrupt, coincident-ON mode occurs with change of direction (PHASE reversal) and/or dynamic braking.

Integrated thermal shutdown protection circuitry switches OFF all power outputs should the junction temperature exceed +165°C (typical). The thermal protection is designed to avoid power IC failures stemming from extreme, excessive junction heating. Thermal shutdown self protection does not afford a proper safeguard from shorted load and/or shorted output conditions, and should not be operated as such. The thermal self-protection circuitry has a (typical) hysteresis of 8°C.

The printed wiring board should utilize a large, heavy ground plane. To optimize power IC performance, the package should be soldered directly into the circuit board. The ground side of $R_S$ should have an individual path to the ground terminal(s) of the device. Also, the load supply ($V_{BB}$) should be closely decoupled with an electrolytic capacitor of between 10 µF and 100 µF (typically ≥47 µF) depending on printed wiring board layout.

**CURRENT CONTROL OPTIONS**

| | Circuit Terminal | | | |
|---|---|---|---|---|
| Control Option | $V_{REF}$/BRAKE | RC (TIMING) | $V_{SENSE}$ | OUTPUT ENABLE |
| No PWM | $V_{CC}$ or High | ≥20 kΩ to Ground | Ground | Low |
| PWM with Internal Timing | $V_{CC}$ or High | $V_{CC}$ | $R_{SENSE}$ | Low |
| PWM with External Timing | 2.4 V or 15 V* or $V_{CC}$ | 20-100 kΩ/200-500 pF | $R_{SENSE}$ | Low |
| External PWM | $V_{CC}$ or High | ≥20 kΩ to Ground | $R_{SENSE}$† | Toggle† |

* Programmed reference, i.e., A/D converter.

† Primarily, closed-loop speed and/or current control applications. $I_{TRIP}$ can be peak (or default) limit for protecting motor and/or driver IC.