

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Octal 3-State Noninverting Transparent Latch

High-Performance Silicon-Gate CMOS

The MC54/74HC573A is identical in pinout to the LS573. The devices are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

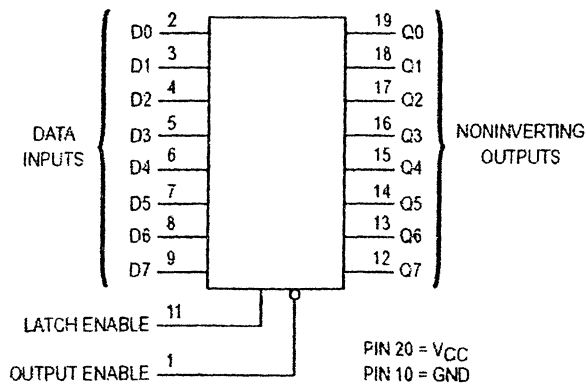
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The HC573A is identical in function to the HCT373A but has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC573A is the noninverting version of the HC563A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates

LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count*	54.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μ W
Speed Power Product	0.0075	pJ

* Equivalent to a two-input NAND gate.

MC54/74HC573A



J SUFFIX
CERAMIC PACKAGE
CASE 732-03



N SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
SOIC PACKAGE
CASE 751D-04



DT SUFFIX
TSSOP PACKAGE
CASE 948E-02

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXADW	SOIC
MC74HCXXXADT	TSSOP

PIN ASSIGNMENT

OUTPUT ENABLE	1	20	VCC
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	LATCH ENABLE

FUNCTION TABLE

Output Enable	Inputs		Output Q
	Latch Enable	D	
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care

Z = High Impedance

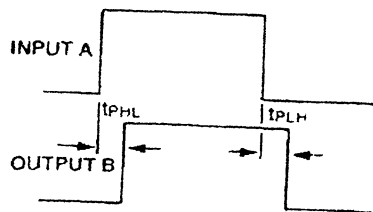
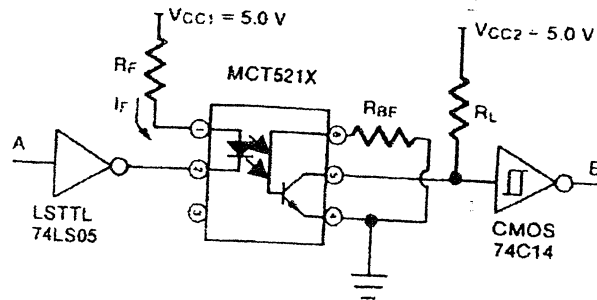
INDIVIDUAL COMPONENT CHARACTERISTICS (T _a = 25°C Unless Otherwise Specified)								
CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS	FIG.	NOTE
INPUT DIODE								
Forward voltage	V _F		1.3	1.5	V	I _F = 5 mA	1	
Forward voltage coefficient	ΔV _F /ΔT _a		-1.9		mV/°C	I _F = 2 mA	1	
Reverse voltage	V _R	5			V	I _R = 10 μA		
Junction capacitance	C _J		18		pF	V _F = 0 V, f = 1 MHz		
			112		pF	V _F = 1 V, f = 1 MHz		
OUTPUT TRANSISTOR								
DC forward current gain	h _{FE(SAT)}		350		—	V _{CE} = 0.4 V, I _{CE} = 2 mA	8,9	
Breakdown voltage Collector to emitter	BV _{CEO}	30	45		V	I _C = 1.0 mA, I _F = 0		
Collector to base	BV _{CBO}	30	70		V	I _C = 10 μA, I _F = 0		
Emitter to base	BV _{EBO}	5	7		V	I _C = 10 μA, I _F = 0		
Leakage current Collector to emitter	I _{CEB}			100	nA	V _{CE} = 10 V, I _F = 0, R _{BE} = 1 MΩ		
Capacitance Collector to emitter	C		10		pF	V _{CE} = 0, f = 1 MHz		
Collector to base			80		pF	V _{CB} = 0, f = 1 MHz		
Emitter to base			15		pF	V _{EB} = 0, f = 1 MHz	11	

TRANSFER CHARACTERISTICS OVER RECOMMENDED TEMPERATURE (T _a = 0°C to 70°C Unless Otherwise Specified)									
CHARACTERISTICS	SYMBOL	DEVICE	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	FIG.	NOTE
Saturated current		MCT5210	60	350		%	I _F = 3.0 mA, V _{CE} = 0.4 V	2	
Transfer ratio (Collector to emitter)	CTR _{CE(SAT)}	MCT5211	100	300		%	I _F = 1.6 mA, V _{CE} = 0.4 V	3	1
			75	250		%	I _F = 1.0 mA, V _{CE} = 0.4 V		
Current transfer ratio (Collector to emitter)	CTR _{CE}	MCT5210	70	400		%	I _F = 3.0 mA, V _{CE} = 5.0 V	5	
		MCT5211	150	350		%	I _F = 1.6 mA, V _{CE} = 5.0 V	4	1
			110	300		%	I _F = 1.0 mA, V _{CE} = 5.0 V		
Current transfer ratio (Collector to base)	CTR _{CB}	MCT5210	0.2	0.9		%	I _F = 3.0 mA, V _{CB} = 4.3 V	6	
		MCT5211	0.3	0.75		%	I _F = 1.6 mA, V _{CB} = 4.3 V	7	2
			0.25	0.6		%	I _F = 1.0 mA, V _{CB} = 4.3 V		
Saturation voltage (Collector to emitter)	V _{CE(SAT)}	MCT5210		0.2	0.4	V	I _F = 3.0 mA, I _{CE} = 1.8 mA		
		MCT5211		0.2	0.4	V	I _F = 1.6 mA, I _{CE} = 1.6 mA		

FAIRCHILD
SEMICONDUCTOR

**HIGH-PERFORMANCE AlGaAs
PHOTOTRANSISTOR OPTOCOUPLEDERS**

TYPICAL ELECTRO-OPTICAL CHARACTERISTICS
($T_A = 25^\circ\text{C}$, Unless Otherwise Specified) (Cont'd)



TYPICAL SWITCHING TIME $T_A = 25^\circ\text{C}$

I_F mA	R_f K Ω	R_L K Ω	R_{RF} K Ω	t_{PHL} μs	t_{PLH} μs	Data K bit/s
1.0	3.3	1.5	=	40	40	12.5
1.0	3.3	10	160	45	45	11
1.6	2.0	750	=	20	20	25
1.6	2.0	4.7	91	25	25	20
3.0	1.1	.33	=	10	10	50
3.0	1.1	3.3	39	12	12	42

C1850

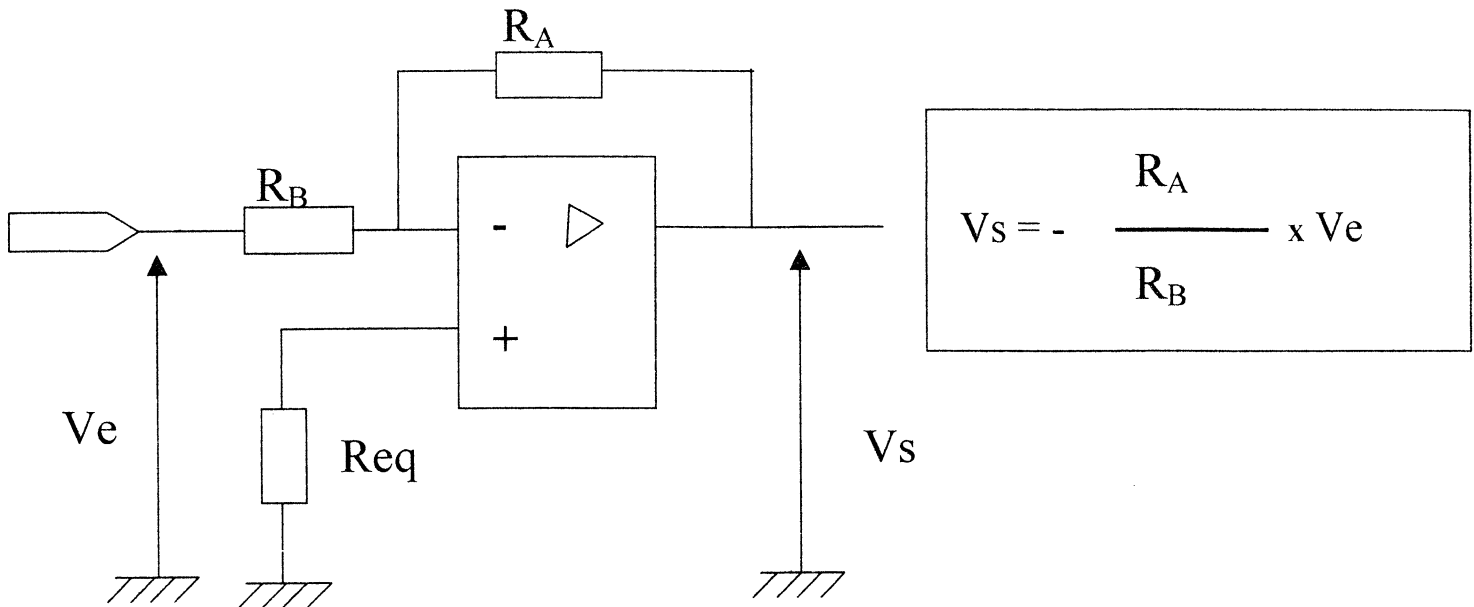
Fig. 13. Switching Speed Test Circuit

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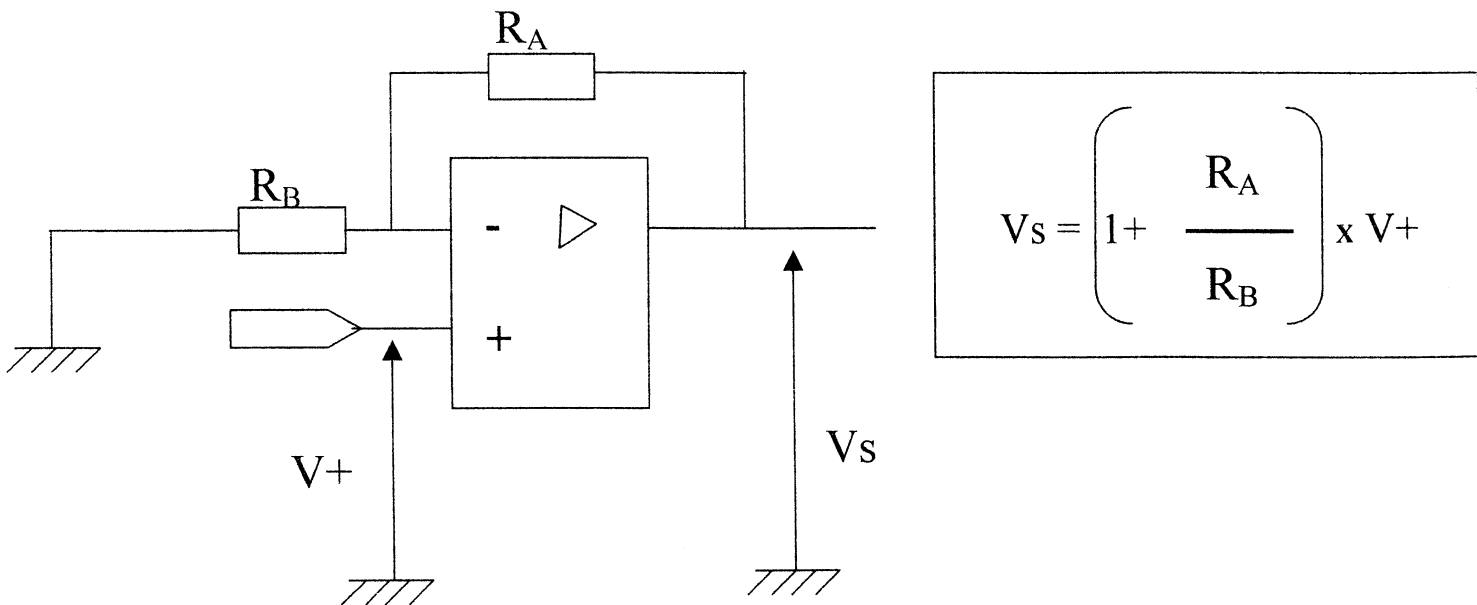
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DOCUMENTS RESSOURCES

AMPLIFICATEUR INVERSEUR EN TENSION



AMPLIFICATEUR NON INVERSEUR EN TENSION



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