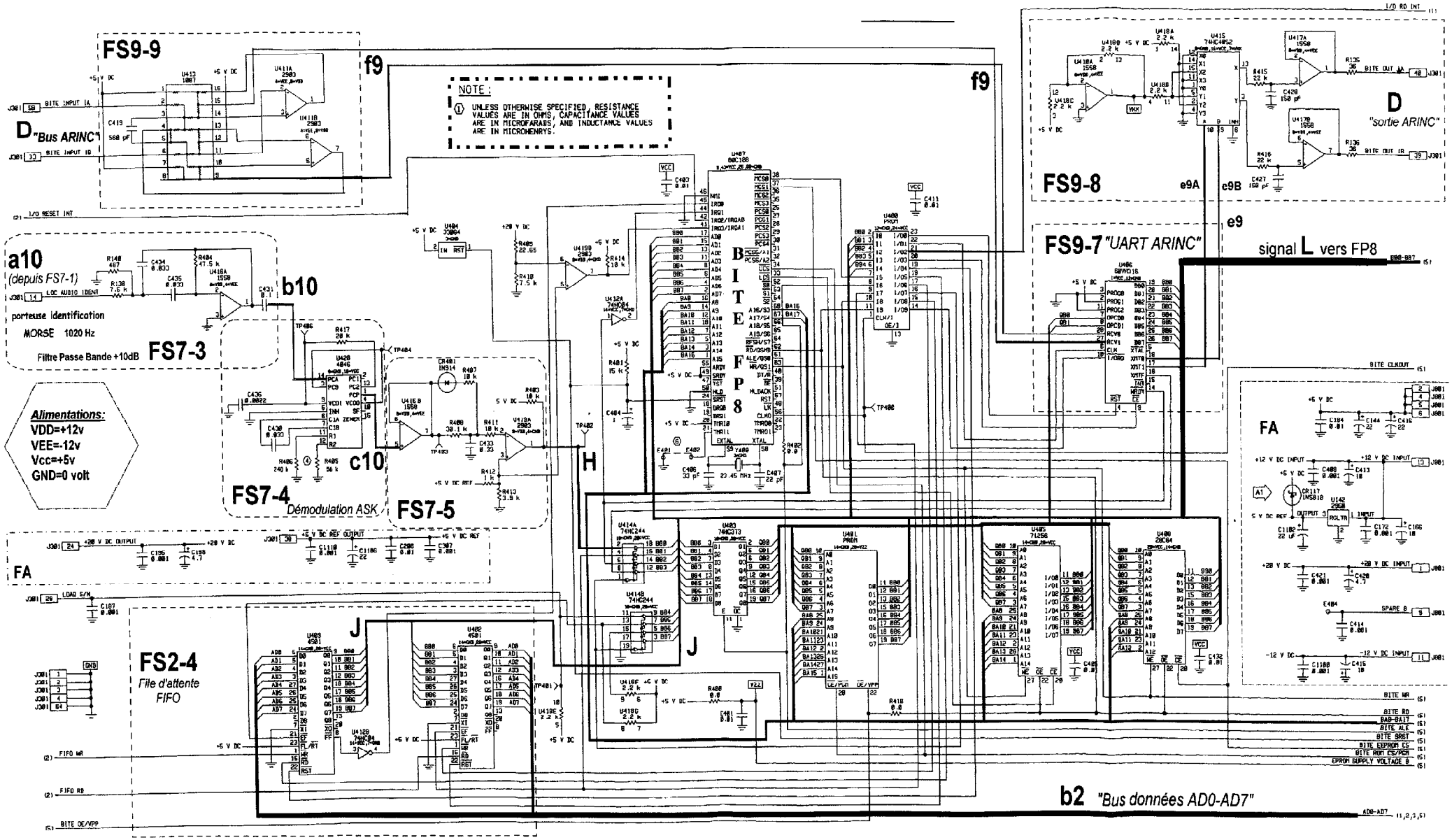
PAGE BLANCHE

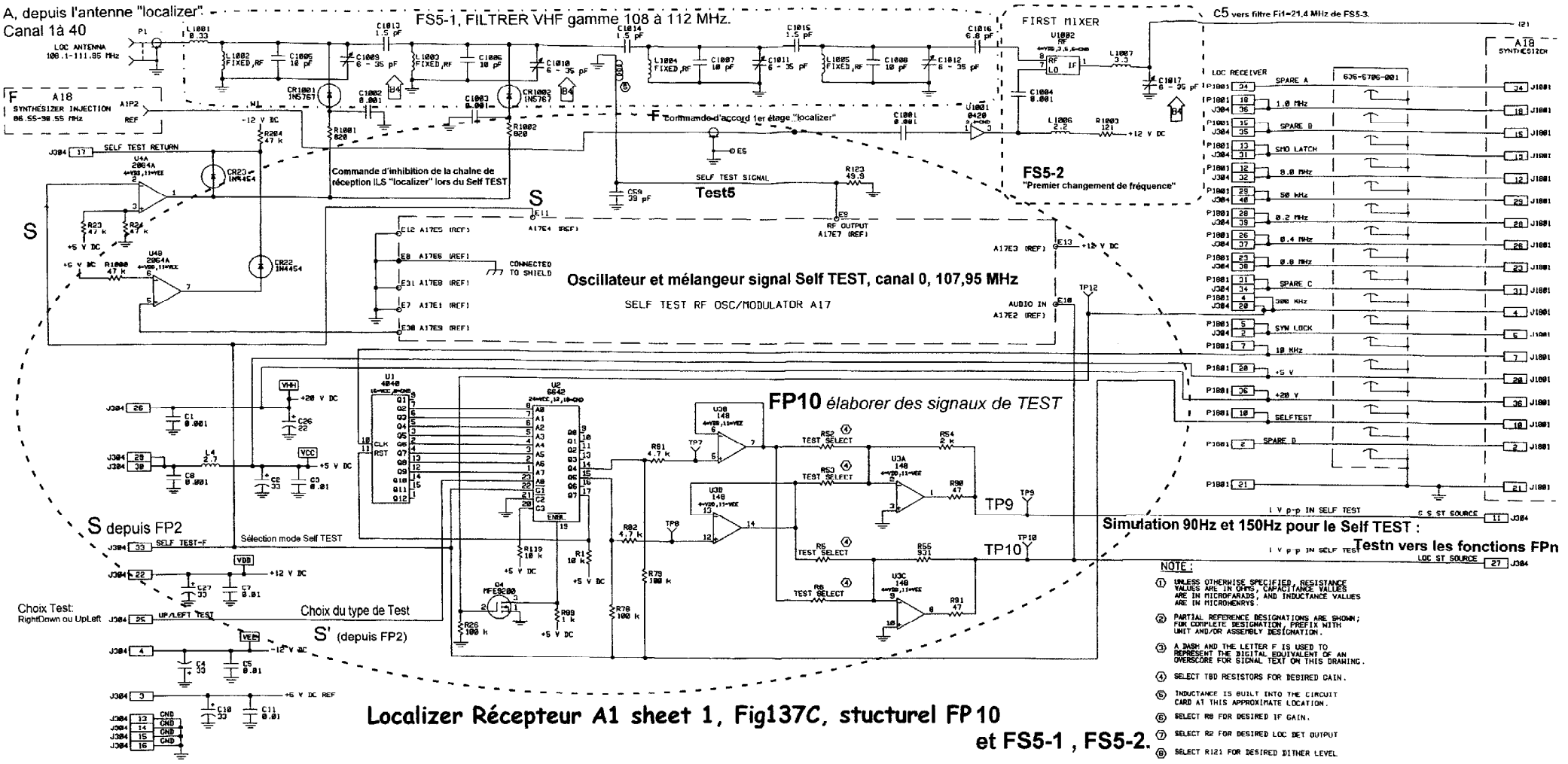
P. *Schéma structurel de FP8 et FS2, FS6 et FS9 partiel : BITE + ident Morse*



BITE I/O Processor A4 sheet 4, Fig152C, stucturel FP 8 et FP7 partiel et FP9 partiel

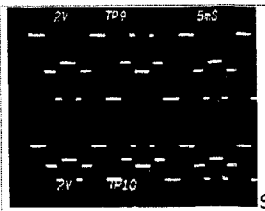
PAGE BLANCHE

Q. Schéma structurel du premier étage du récepteur « localizer » FS5-1, FS5-2 et « Self Test » FP10

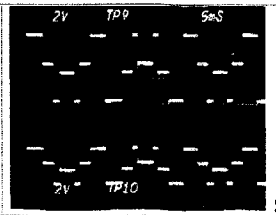


*Ci-contre, exemples d'oscillogrammes relevés aux points **TP9** et **TP10**, en mode Self TEST.*

Les signaux à 90 Hz et 150 Hz sont mélangés avec des amplitudes différentes de façon à émuler une position de l'aéronef par rapport à la trajectoire de consigne, soit :
** DownRight : en Bas et à Droite de la trajectoire de consigne.*
** UpLeft : en Haut et à Gauche.*



S'=0 DownRight Self TEST



S'=1 UpLeft Self TEST

Fin du Dossier Technique : Récepteur ILS.

B.T.S. ELECTRONIQUE

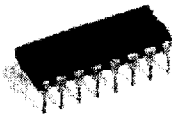
SESSION 2004

ETUDE D'UN SYSTEME TECHNIQUE

Système d'aide à l'atterrissage

Quelques composants du Récepteur I.L.S.

Dossier documentation Constructeur.



Ce dossier comporte 32 pages.

SGS-THOMSON MICROELECTRONICS

HCC/HCF4018B

PRESETTABLE DIVIDE-BY-N COUNTER

- MEDIUM SPEED OPERATION - 10MHz (typ.) AT $V_{DD} - V_{SS} = 10V$
- FULLY STATIC OPERATION
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

EY
(Plastic Package)

F
(Ceramic Frit Seal Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

HCC4018BF	HCF4018BM1
HCF4018BEY	HCF4018BC1

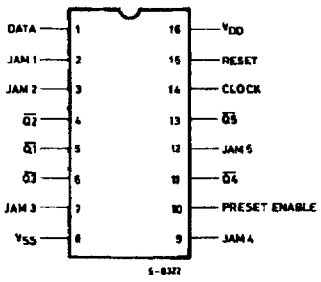
DESCRIPTION

The HCC4018B (extended temperature range) and **HCF4018B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4018B** types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the Q5, Q4, Q3, Q2, Q1 signals, respectively, back to the DATA input.

Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a **HCC/HCF4011B** gate package to properly gate the feedback connection to the DATA input. Divide-by-functions greater than 10 can be achieved by use of multiple **HCC/HCF 4018B** units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESENT-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

PIN CONNECTIONS



TYPICAL APPLICATIONS

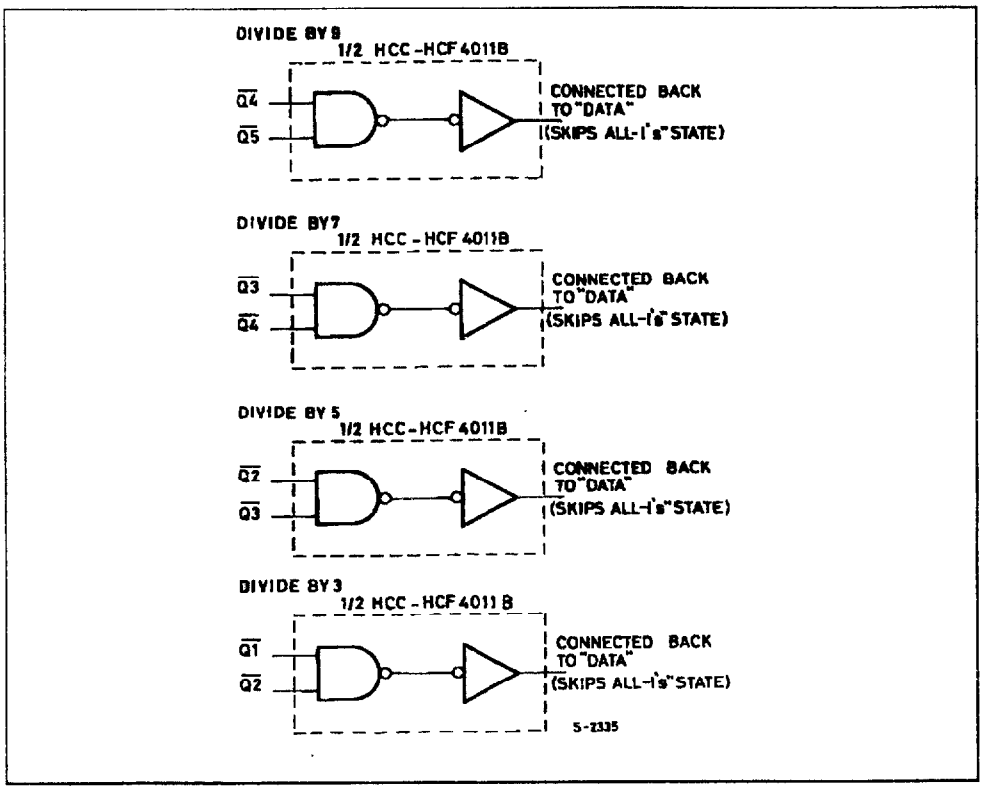
External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

DIVIDE BY 10 Q_5
DIVIDE BY 8 Q_4
DIVIDE BY 6 Q_3
DIVIDE BY 4 Q_2
DIVIDE BY 2 Q_1

CONNECTED BACK TO "DATA"

NO CONNECTED

NO EXTERNAL COMPONENTS REQUIRED

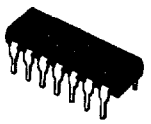


SGS-THOMSON MICROELECTRONICS

HCC/HCF4013B

DUAL 'D' – TYPE FLIP–FLOP

- SET-RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM-SPEED OPERATION - 16MHz (typ.) CLOCK TOGGLE RATE AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)

F
(Ceramic Frit Seal Package)

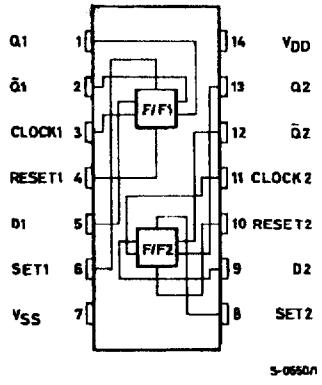
M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

HCC4013BF	HCF4013BM1
HCF4013BEY	HCF4013BC1

PIN CONNECTIONS



DESCRIPTION

The **HCC4013B** (extended temperature range) and **HCF4013B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4013B** consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the $\overline{Q}$ output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

HCC/HFC4013B

ABSOLUTE MAXIMUM RATINGS

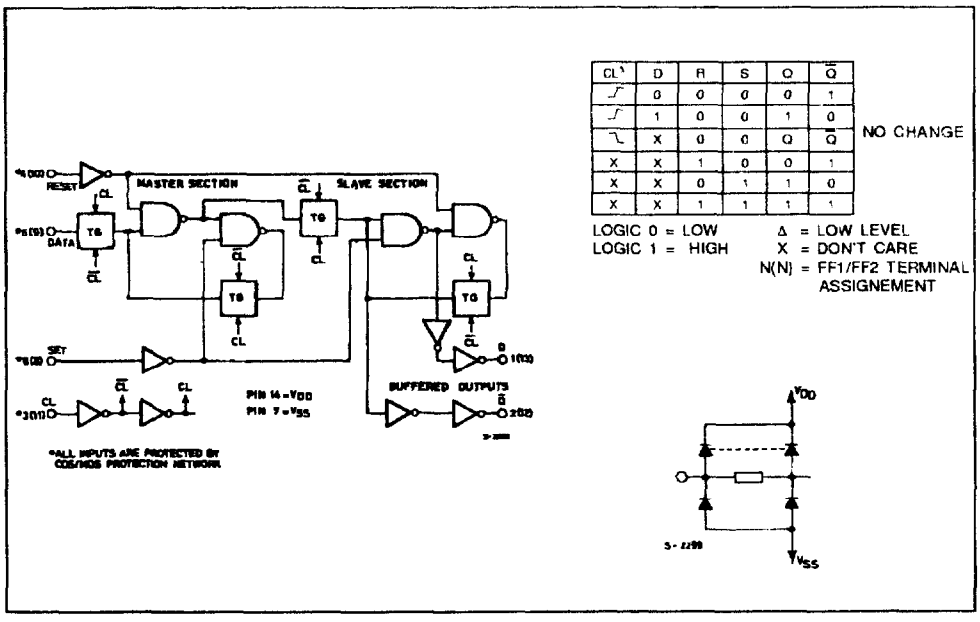
Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : **HCC** Types **HCF** Types	− 0.5 to + 20 − 0.5 to + 18	V V
V_I	Input Voltage	− 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	− 55 to + 125 − 40 to + 85	°C °C
T_{stg}	Storasge Temperature	− 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltages are with respect to V_{SS} (GND).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : **HCC** Types **HCF** Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	− 55 to + 125 − 40 to + 85	°C °C

LOGIC DIAGRAM AND TRUTH TABLE (one of two identical flip–flops)



CL	D	R	S	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

NO CHANGE

LOGIC 0 = LOW
LOGIC 1 = HIGH
Δ = LOW LEVEL
X = DON'T CARE
N(N) = FF1/FF2 TERMINAL ASSIGNEMENT

Dual 4-channel analogue multiplexer/demultiplexer

HEF4052B
MSI

DESCRIPTION

The HEF4052B is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (Y_0 to Y_3) and a common input/output (Z). The common channel select logic includes two address inputs (A_0 and A_1) and an active LOW enable input ($\overline{E}$).

Both multiplexers/demultiplexers contain four bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_3) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by A_0 and A_1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 and A_1.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0, A_1 and $\overline{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_3, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

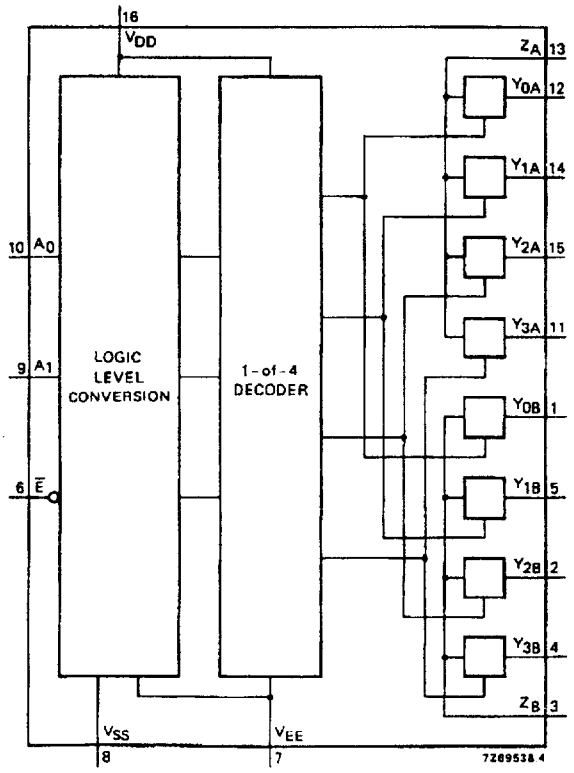


Fig.1 Functional diagram.

PINNING

Y_{0A} to Y_{3A}	independent inputs/outputs
Y_{0B} to Y_{3B}	independent inputs/outputs
A_0, A_1	address inputs
$\overline{E}$	enable input (active LOW)
Z_A, Z_B	common inputs/outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

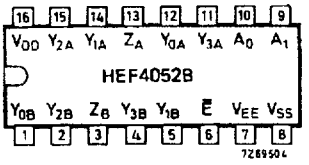


Fig.2 Pinning diagram.

HEF4052BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4052BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4052BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

National Semiconductor

August 1989

MM54HC4051/MM74HC4051 8-Channel Analog Multiplexer MM54HC4052/MM74HC4052 Dual 4-Channel Analog Multiplexer MM54HC4053/MM74HC4053 Triple 2-Channel Analog Multiplexer

MM54/74HC4051 8-Channel, MM54/74HC4052 Dual 4-Channel and MM54/74HC4053 Triple 2-Channel Analog Multiplexers

General Description

These multiplexers are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for V_{CC}, ground, and V_{EE}. This enables the connection of 0–5V logic signals when V_{CC} = 5V and an analog input range of ±5V when V_{EE} = 5V. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4051/MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is "on", and connects one of the eight inputs to the common output.

MM54HC4052/MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4-channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4-channel differential multiplexer.

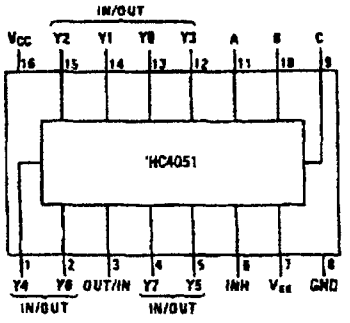
MM54HC4053/MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configurations. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

Features

- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. (V_{CC}–V_{EE} = 4.5V)
  30 typ. (V_{CC}–V_{EE} = 9V)
- Logic level translation to enable 5V logic with ±5V analog signals
- Low quiescent current: 80 μA maximum (74HC)
- Matched Switch characteristic

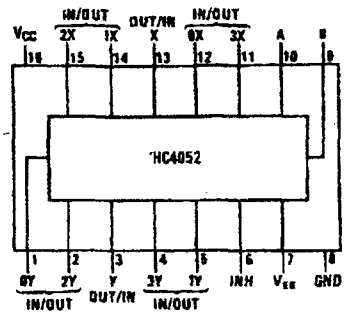
Connection Diagrams

Dual-In-Line Packages



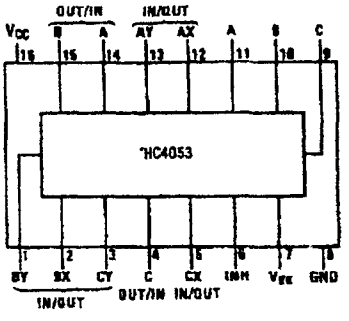
TL/F/5353–1

Top View



TL/F/5353–2

Top View



TL/F/5353–3

Top View

Order Number MM54HC4051, MM74HC4051, MM54HC4052, MM74HC4052, MM54HC4053 or MM74HC4053

RRD-B30M105/Printed in U. S. A.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V–6V, C_L = 50 pF (unless otherwise specified) (Continued)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C		54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits			
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input 4051 Common 4052 Common 4053 Common			15 90 45 30				pF
C_{IN}	Maximum Feedthrough Capacitance				5				pF

Truth Tables

'4051

Input				"ON" Channel
Inh	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

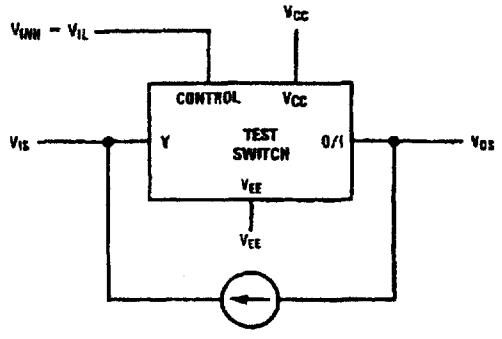
'4052

Inputs			"ON" Channels	
Inh	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

'4053

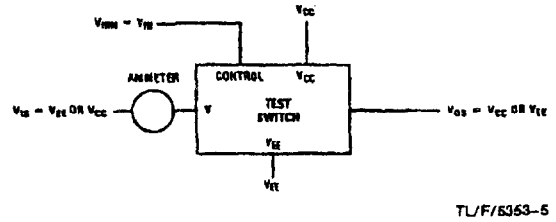
Input				"ON" Channels		
Inh	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AX
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AX
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AX
L	H	H	H	CY	BY	AY

AC Test Circuits and Switching Time Waveforms



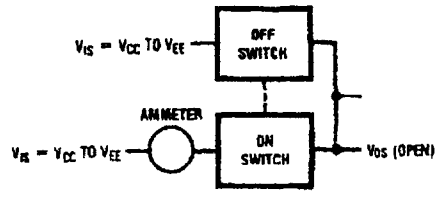
TL/F/5353–4

FIGURE 1. "ON" Resistance



TL/F/5353–5

FIGURE 2. "OFF" Channel Leakage Current



TL/F/5353–6

FIGURE 3. "ON" Channel Leakage Current

ANALOG DEVICES

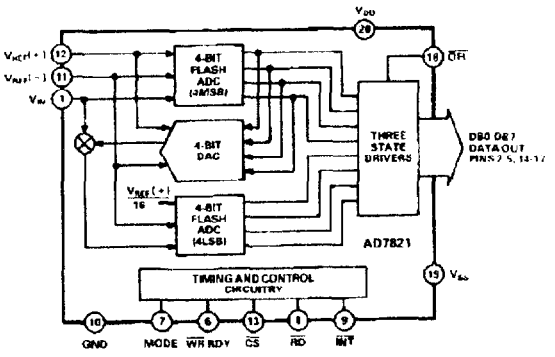
LC²MOS High Speed, µP-Compatible 8-Bit ADC with Track/Hold Function

AD7821

FEATURES

Fast Conversion Time: 660 ns max
100 kHz Track-and-Hold Function
1 MHz Sample Rate
Unipolar and Bipolar Input Ranges
Ratiometric Reference Inputs
No External Clock
Extended Temperature Range Operation
Skinny 20-Pin DIPs, SOIC and 20-Terminal *Surface Mount Packages*

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7821 is a high speed, 8-bit, sampling, analog-to-digital converter that offers improved performance over the popular AD7820. It offers a conversion time of 660 ns (vs. 1.36 µs for the AD7820) and 100 kHz signal bandwidth (vs. 6.4 kHz). The sampling instant is better defined and occurs on the falling edge of $\overline{WR}$ or $\overline{RD}$. The provision of a V_{SS} pin (Pin 19) allows the part to operate from ±5 V supplies and to digitize bipolar input signals. Alternatively, for unipolar inputs, the V_{SS} pin can be grounded and the AD7821 will operate from a single +5 V supply, like the AD7820.

The AD7821 has a built-in track-and-hold function capable of digitizing full-scale signals up to 100 kHz max. It also uses a half-flash conversion technique that eliminates the need to generate a CLK signal for the ADC.

The AD7821 is designed with standard microprocessor control signals ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and latched, three-state data outputs capable of interfacing to high speed data buses. An overflow output ($\overline{OFL}$) is also provided for cascading devices to achieve higher resolution.

The AD7821 is fabricated in Linear-Compatible CMOS (LC²MOS), an advanced, mixed technology process combining precision bipolar circuits with low power CMOS logic. The part features a low power dissipation of 50 mW.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC²MOS process, enables a very fast conversion time. The conversion time for the WR-RD mode is 660 ns, with 700 ns for the RD mode.
2. Built-In Track-and-Hold
   This allows input signals with slew rates up to 1.6 V/µs to be converted to 8-bits without an external track-and-hold. This corresponds to a 5 V peak-to-peak, 100 kHz sine wave signal.
3. Total Unadjusted Error
   The AD7821 features an excellent total unadjusted error figure of less than ±1 LSB over the full operating temperature range.
4. Unipolar/Bipolar Input Ranges
   The AD7821 is specified for single supply (+5 V) operation with a unipolar full-scale range of 0 to +5 V, and for dual supply (±5 V) operation with a bipolar input range of ±2.5 V. Typical performance characteristics are given for other input ranges.
5. Dynamic Specifications for DSP Users
   In addition to the traditional ADC specifications, the AD7821 is specified for ac parameters, including signal-to-noise ratio, distortion and slew rate.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD7821–SPECIFICATIONS

V_{DD} = +5 V ± 5%, GND = 0 V. Unipolar Input Range: V_{SS} = GND, $V_{REF}(+)$ = 5 V, $V_{REF}(-)$ = GND. Bipolar Input Range: V_{SS} = −5 V ± 5%, $V_{REF}(+)$ = 2.5 V, $V_{REF}(-)$ = −2.5 V. These test conditions apply unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted. Specifications apply for PD Mode (Pin 7 = 0 V).

Parameter	K Version[1]	B, T Versions	Units	Comments
UNIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Total Unadjusted Error[3]	±1	±1	LSB max	
Minimum Resolution for which No Missing Codes are Guaranteed	8	8	Bits	
BIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Zero Code Error	±1	±1	LSB max	
Full Scale Error	±1	±1	LSB max	
Signal-to-Noise Ratio (SNR)[3]	45	45	dB min	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Total Harmonic Distortion (THD)[3]	−50	−50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Peak Harmonic or Spurious Noise[3]	−50	−50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Intermodulation Distortion (IMD)[3]				fa (84.72 kHz) and fb (94.97 kHz) Full-Scale Sine Waves with $f_{SAMPLING}$ = 500 kHz
	−50	−50	dB max	Second Order Terms
	−50	−50	dB max	Third Order Terms
Slew Rate, Tracking[3]	1.6	1.6	V/µs max	
	2.36	2.36	V/µs typ	
REFERENCE INPUT				
Input Resistance	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(-)/V_{DD}$	$V_{REF}(-)/V_{DD}$	V min/V max	
$V_{REF}(-)$ Input Voltage Range	$V_{SS}/V_{REF}(+)$	$V_{SS}/V_{REF}(+)$	V min/V max	
ANALOG INPUT				
Input Voltage Range	$V_{REF}(-)/V_{REF}(+)$	$V_{REF}(-)/V_{REF}(+)$	V min/ max	
Input Leakage Current	±3	±3	µA max	−5 V ≤ V_{IN} ≤ +5 V
Input Capacitance	55	55	pF typ	
LOGIC INPUTS				
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$				
V_{INH}	2.4	2.4	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	µA max	
I_{INH} ($\overline{WR}$)	3	3	µA max	
I_{INL}	−1	−1	µA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
MODE				
V_{INH}	3.5	3.5	V min	
V_{INL}	1.5	1.5	V max	
I_{INH}	200	200	µA max	50 µA typ
I_{INL}	−1	−1	µA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
LOGIC OUTPUTS				
DB0–DB7, $\overline{OFL}$, $\overline{INT}$				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 360 µA
V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
I_{OUT} (DB0–DB7)	±3	±3	µA max	Floating State Leakage
Output Capacitance[4] (DB0–DB7)	8	8	pF max	Typically 5 pF
RDY				
V_{OL}	0.4	0.4	V max	I_{SINK} = 2.0 mA
I_{OUT}	±3	±3	µA max	Floating State Leakage
Output Capacitance[4]	8	8	pF max	Typically 5 pF
POWER SUPPLY				
I_{DD}[5]	15	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
I_{SS}	100	100	µA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
Power Dissipation	50	50	mW typ	
Power Supply Sensitivity	±1/4	±1/4	LSB max	±1/16 LSB typ, V_{DD} = 4.75 V to 5.25 V, ($V_{REF}(+)$ = 4.75 V max for Unipolar Mode)

NOTES

[1]Temperature Ranges are as follows: K Version = −40°C to +85°C; B Version = −40°C to +85°C; T Version = −55°C to +125°C.

[2]1 LSB = 19.53 mV for both the unipolar (0 V to +5 V) and bipolar (−2.5 V to +2.5 V) input ranges.

[3]See Terminology.

[4]Sample tested at +25°C to ensure compliance.

[5]See Typical Performance Characteristics.

Specifications subject to change without notice.

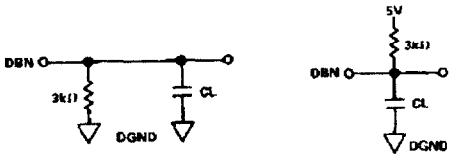
TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = 0 V or −5 V ± 5%; Unipolar or Bipolar Input Range)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (K, B Versions)	Limit at T_{MIN}, T_{MAX} (T Version)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time
t_{RDY}[2]	70	85	100	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5 kΩ.
t_{CRD}	700	875	975	ns max	Conversion Time (RD Mode)
t_{ACC0}[3]					Data Access Time (RD Mode)
	t_{CRD} + 25	t_{CRD} + 30	t_{CRD} + 35	ns max	C_L = 20 pF
	t_{CRD} + 50	t_{CRD} + 65	t_{CRD} + 75	ns max	C_L = 100 pF
t_{INTR}[2]	50	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	80	85	90	ns max	
t_{DH}[4]	15	15	15	ns min	Data Hold Time
	60	70	80	ns max	
t_P	350	425	500	ns min	Delay Time Between Conversions
t_{WR}	250	325	400	ns min	Write Pulse Width
	10	10	10	µs max	
t_{RD}	250	350	450	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{READ1}	160	205	240	*ns min*	$\overline{RD}$ Pulse Width (WR-RD Mode, see Figure 12b) Determined by t_{ACC1}
t_{ACC1}[3]					Data Access Time (WR-RD Mode, see Figure 12b)
	160	205	240	ns max	C_L = 20 pF
	185	235	275	ns max	C_L = 100 pF
t_{RI}	150	185	220	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	380	–	–	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	500	610	700	ns max	
t_{READ2}	65	75	85	ns min	$\overline{RD}$ Pulse Width (WR-RD Mode, see Figure 12a) Determined by t_{ACC2}
t_{ACC2}[3]					Data Access Time (WR-RD Mode, see Figure 12a)
	65	75	85	ns max	C_L = 20 pF
	90	110	130	ns max	C_L = 100 pF
t_{HWR}[2]	80	100	120	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}[5]					Data Access Time after $\overline{INT}$ (Stand-Alone Operation)
	30	35	40	ns max	C_L = 20 pF
	45	60	70	ns max	C_L = 100 pF

NOTES
[1]Sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]C_L = 50 pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

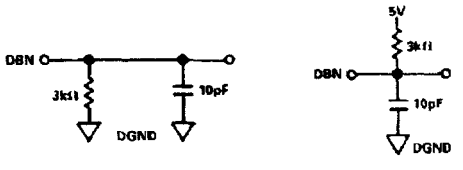
Specifications subject to change without notice.

Test Circuits



a. High Z to V_{OH} *b. High Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High Z *b. V_{OL} to High Z*

Figure 2. Load Circuits for Data Hold Time Test

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7821KN	–40°C to +85°C	±1 max	N-20
AD7821KP	–40°C to +85°C	±1 max	P-20A
AD7821KR	–40°C to +85°C	±1 max	R-20
AD7821BQ	–40°C to +85°C	±1 max	Q-20
AD7821TQ	–55°C to +125°C	±1 max	Q-20
AD7821TE	–55°C to +125°C	±1 max	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

AD7821

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND ..... –0.3 V, + 7 V
V_{SS} to GND ..... +0.3 V, + 7 V
Digital Input Voltage to GND
(Pins 6–8, 13) ..... –0.3 V, V_{DD} + 0.3 V
Digital Output Voltage to GND
(Pins 2–5, 9, 14–18) ..... –0.3 V, V_{DD} + 0.3 V
V_{REF}(+) to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{REF}(–) to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{IN} to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
Commercial (K Version) ..... –40°C to +85°C
Industrial (B Version) ..... –40°C to +85°C
Extended (T Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates above +75°C by ..... 6 mW/°C

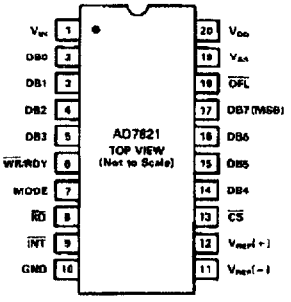
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

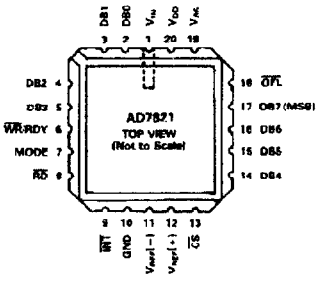
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7821 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

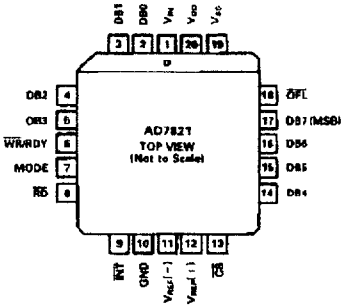
DIP AND SOIC



LCCC



PLCC



TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 8-bit resolution can resolve one part in 2^8 (1/256 of full scale). For the AD7821 operating in either the unipolar or bipolar input range with 5 V full scale, one LSB is 19.53 mV.

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes relative accuracy, offset error and full-scale error.

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error.

TOTAL HARMONIC DISTORTION

Total harmonic distortion is the ratio of the square root of the sum of the squares of the rms value of the harmonics to the rms value of the fundamental. For the AD7821, total harmonic distortion (THD) is defined as

$$20\ log\left[\frac{\sqrt{\left(V_2^2+V_3^2+V_5^2+V_6^2\right)}}{V_1}\right] dB$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6, are the rms amplitudes of the individual harmonics.

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa+nfb, where m, n = 0, 1, 2, 3,- - - -. Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), and the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). For the AD7821 intermodulation distortion is calculated separately for both the second and third order terms.

SIGNAL-TO-NOISE RATIO

Signal-to-noise ratio (SNR) is measured signal-to-noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals (excluding dc) up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process. The theoretical SNR for a sine wave input is given by:

$$SNR = (6.02\ N + 1.76)\ dB$$

where N is the number of bits in the ADC. Thus, for an ideal 8-bit ADC, SNR = 50 dB.

PEAK HARMONIC OR SPURIOUS NOISE

Peak harmonic or spurious noise is the rms value of the largest nonfundamental frequency (excluding dc) up to half the sampling frequency to the rms value of the fundamental.

AD7821

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{IN}	Analog Input: Range $V_{REF}(-) \le V_{IN} \le V_{REF}(+)$
2	DB0	Three-State Data Output (LSB).
3–5	DB1–DB3	Three-State Data Outputs.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. This input is internally pulled low through a 50 µA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$. See Digital Interface section.
10	GND	Ground.
11	$V_{REF}(-)$	Lower limit of reference span. Range: $V_{SS} \le V_{REF}(-) \le V_{REF}(+)$.
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) < V_{REF}(+) \le V_{DD}$.
13	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
14–16	DB4–DB6	Three-State Data Outputs.
17	DB7	Three-State Data Output (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+)$ – 1/2 LSB), $\overline{OFL}$ will be low at the end of conversion. It is a non-three-state output which can be used to cascade 2 or more devices to increase resolution.
19	V_{SS}	Negative supply voltage. V_{SS} = 0 V; Unipolar Operation. V_{SS} = –5 V; Bipolar Operation.
20	V_{DD}	Positive supply voltage, +5 V.

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7821 uses a half flash conversion technique (see Functional Block Diagram), whereby two 4-bit flash ADCs are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators, which compare an unknown input voltage to the reference ladder, to achieve a 4-bit result. The MS (most significant) flash ADC converts an unknown analog input voltage (V_{IN}) to provide the 4 MS data bits. An internal DAC, driven by the 4 MS data bits, then recreates an analog approximation of the input voltage. The DAC output voltage is subtracted from the analog input, and the difference is converted by the LS (least significant) ADC to provide the 4 LS data bits. The MS flash ADC also has one additional comparator to detect overrange on the analog input.

OPERATING SEQUENCE

The AD7821 has two operating modes. The RD mode allows a conversion to be started and data to be read with a single, extended, READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low). The conversion process is timed out by internal one-shots. The WR-RD mode uses $\overline{WR}$ to start a conversion and $\overline{RD}$ to read the data and allows the conversion timing to be externally controlled. The operating sequence for the WR-RD mode is shown in Figure 3.

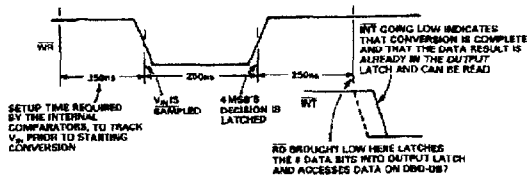


Figure 3. Operating Sequence (WR-RD Mode)

A conversion is initiated and the analog input signal (V_{IN}) sampled on the falling edge of $\overline{WR}$ (falling edge of $\overline{RD}$, RD mode). A setup time (t_P, delay time between conversions) of 350 ns is required prior to this falling edge. See Digital Interface section for more details. When $\overline{WR}$ is low, the internal MS (most significant) ADC compares the sampled analog input with the reference ladder to provide the 4 MS data bits. A minimum of 250 ns is required for this comparison. On the rising edge of $\overline{WR}$, the MS data result is latched internally and the LS (least significant) conversion begins, to yield the 4 LS data bits. $\overline{INT}$ goes low typically 380 ns after the rising edge of $\overline{WR}$. This indicates the LS conversion is complete and that both the LS and MS data results are latched into the output buffer. $\overline{RD}$ going low then enables the output data. If a faster conversion time is required, the $\overline{RD}$ line can be brought low 250 ns after $\overline{WR}$ goes high. This latches both the LS and MS data bits and outputs the conversion result on DB0–DB7.

REFERENCE AND INPUT

The $V_{REF}(-)$ and $V_{REF}(+)$ reference inputs on the AD7821 are fully differential and define the zero and full-scale input range of the ADC. The transfer characteristic of the part is defined by the integer value of the following expression:

$$Data\ (LSBs) = 256\left[\frac{V_{IN} - V_{REF}(-)}{V_{REF}(+) - V_{REF}(-)}\right] + 0.5$$

As a result, the analog input (V_{IN}) Of the device can easily be set up to provide both unipolar and bipolar operation. The data output code for unipolar and bipolar operation is Natural Binary and Offset Binary, respectively.

The span of the analog input voltage can easily be varied. By reducing the reference span, $V_{REF}(+) - V_{REF}(-)$, to less than 5 V the sensitivity of the converter can be increased (i.e., if V_{REF} = 2 V then 1 LSB = 7.8 mV). The reference flexibility also allows the input span for unipolar operation to be offset from zero ($V_{REF}(-) > GND$). Additionally, the input/reference arrangement facilitates ratiometric operation.

Figures 4 and 5 show some configurations which are possible. For minimum noise a 47 µF capacitor in parallel with a 0.1 µF capacitor should be connected between the reference inputs and GND.