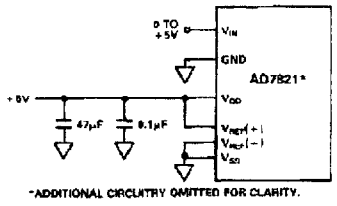


Figure 4. Power Supply as Reference. Unipolar Operation (0 to + 5 V)

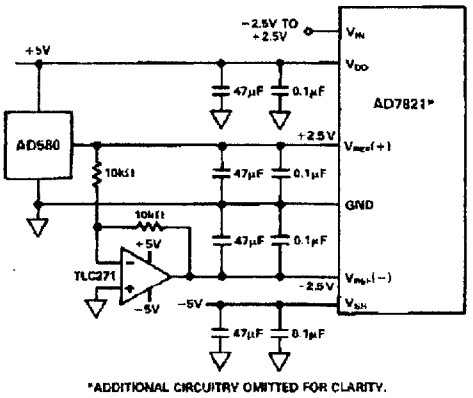


Figure 5. External Reference. Bipolar Operation (−2.5 V to +2.5 V)

INPUT CURRENT

The analog input of the AD7821 behaves somewhat differently to conventional A/D converters. This is due to the ADC's sampled data comparators, which take varying amounts of input current depending on the cycle of the converter.

The equivalent input circuit of the AD7821 is shown in Figure 6. When a conversion ends (e.g., falling edge of $\overline{INT}$, WR-RD mode, $t_{RD} > t_{INTL}$) all the input switches are closed and V_{IN} is connected to the comparators of the internal LS and MS ADCs. Therefore, V_{IN} is connected to 31 one-pF input capacitors simultaneously.

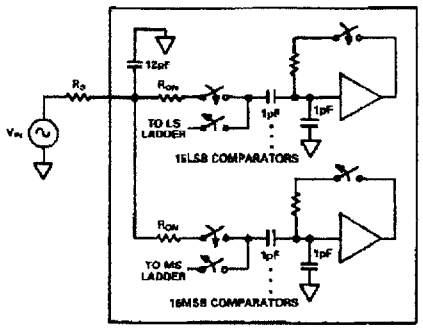


Figure 6. AD7821 Equivalent Input Circuit

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2 kΩ to 5 kΩ). In addition, about 12 pF of input stray capacitance must be charged.

The analog input can be modeled as an equivalent RC network as shown in Figure 7. As R_S (source impedance) increases, the input capacitance takes longer to charge.

The comparators track the analog input between conversions. A minimum delay time (t_P) of 350 ns is required between conversions to allow for voltage source settling and comparator tracking time. This allows input time constants of 50 ns without settling time problems. Typical total input capacitance values of 55 pF allow R_S to be 0.9 kΩ without lengthening t_P to give V_{IN} more time to settle.

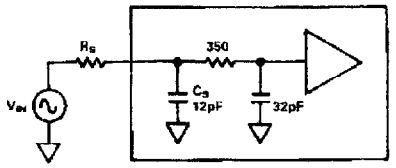


Figure 7. RC Network Model

INPUT TRANSIENTS

Transients on the analog input signal caused by charging current flowing into V_{IN} will not normally degrade the ADC's performance. In effect, the AD7821 does not "look" at the input when these transients occur. The comparators' inputs track V_{IN} and are not sampled until the falling edge of $\overline{WR}$ (WR-RD Mode) or $\overline{RD}$ (RD Mode), so at least 350 ns (t_P) is provided to charge the ADC's input capacitance. It is, therefore, not necessary to filter out these transients with an external capacitor at the V_{IN} terminal.

INHERENT TRACK-AND-HOLD

A major benefit of the AD7821's input structure is its ability to measure a variety of high-speed signals without the help of an external track-and-hold. Any ADC which does not have a built-in track-and-hold, regardless of its speed, requires the analog input to remain stable to at least 1/2 LSB for the duration of the conversion to maintain full accuracy. This requires the use of a track-and-hold whenever the input is a high-speed signal. The AD7821's sampled-data comparators, by nature of their input switching, inherently accomplish this track-and-hold function. Although the conversion time for the AD7821 is 660 ns (WR-RD mode, $t_{WR} + t_{RD} + t_{ACC1}$), the time for which V_{IN} must be stable to 1/2 LSB is much smaller. The AD7821 tracks V_{IN} between conversions only, and its value on the falling edge of $\overline{WR}$ or $\overline{RD}$ in the WR-RD or RD modes, respectively, is the measured value.

SINUSOIDAL INPUTS

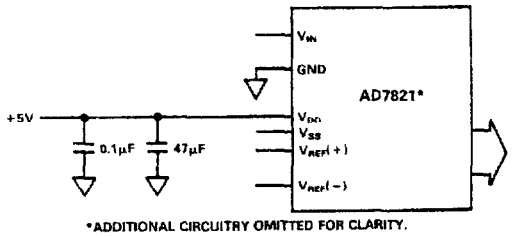
The bandwidth of the built-in track-and-hold is 100 kHz max (150 kHz typ, 5 V p-p). This is limited by the analog bandwidth of the comparators and timing skew between the comparator switches. This means that the analog input frequency can be up to 100 kHz without the aid of an external track-and-hold. The Nyquist criterion requires that the sampling rate be at least twice the input frequency (i.e., ≥2 × 100 kHz). This requires an ideal antialiasing filter with an infinite roll-off. To ease the prob-

APPLYING THE AD7821

The AD7821 is specified for a unipolar input range of 0 to +5 V and a bipolar input range of -2.5 V to +2.5 V. The $V_{REF}(-)$ and $V_{REF}(+)$ voltages required for these input ranges are outlined below. See the Typical Performance Characteristics section for operation with unspecified input voltage ranges.

UNIPOLAR OPERATION

Figure 18 gives the configuration and reference voltages required for 0 V to +5 V operation. The nominal transfer characteristic for this input range is shown in Figure 19. The output code is Natural Binary with 1 LSB = (5/256) V = 19.5 mV.



*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

$V_{REF}(+)$	$V_{REF}(-)$	V_{SS}	V_{IN}	RANGE
+5V	GND	GND	UNIPOLAR	0 to +5V
+2.5V	−2.5V	−5V	BIPOLAR	−2.5V to +2.5V

Figure 18. AD7821 Unipolar/Bipolar Operation

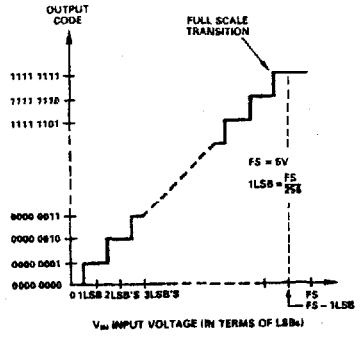


Figure 19. Nominal Transfer Characteristic for Unipolar (0 V to +5 V) Operation

BIPOLAR OPERATION

Figure 18 gives the configuration and reference voltages required for -2.5 V to +2.5 V operation. The nominal transfer characteristic for this input range is shown in Figure 20. The output code is Offset Binary with 1 LSB = ([+2.5 - (-2.5)]/256) V = 19.5 mV.

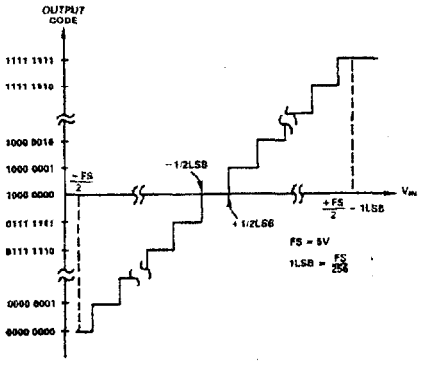


Figure 20. Nominal Transfer Characteristic for Bipolar (-2.5 V to +2.5 V) Operation

16-CHANNEL TELECOM A/D CONVERTER

The fast sampling rate (1 MHz) and bipolar operation of the AD7821 makes it useful in Telecom applications for sampling a number of input channels using a multiplexer. Figure 21 shows a circuit for such an application.

The maximum signal frequency required for acceptable quality in Telecom applications is 3 kHz. The circuit given in Figure 21 permits each of the 16-input channels to be sampled at a rate of 16 kHz maximum. The sampling rate takes account of such multiplexer parameters as t_{ON}, settling time etc. The circuit also eases the problem of the antialiasing filter design by sampling at a rate much greater than that required by the Nyquist criterion.

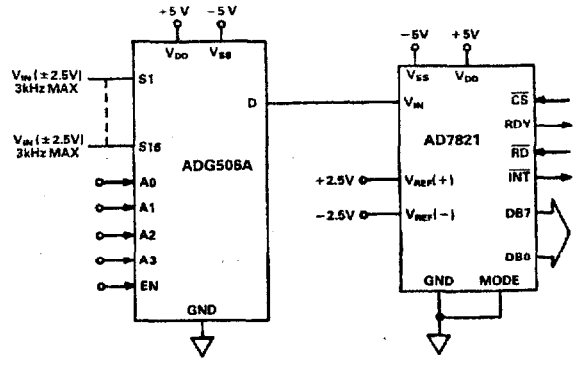


Figure 21. 16-Channel Telecom A/D Converter System

Phase-locked loop

HEF4046B
MSI

DESCRIPTION

The HEF4046B is a phase-locked loop circuit that consists of a linear voltage controlled oscillator (VCO) and two different phase comparators with a common signal input amplifier and a common comparator input. A 7 V regulator (zener) diode is provided for supply voltage regulation if necessary. For functional description see further on in this data.

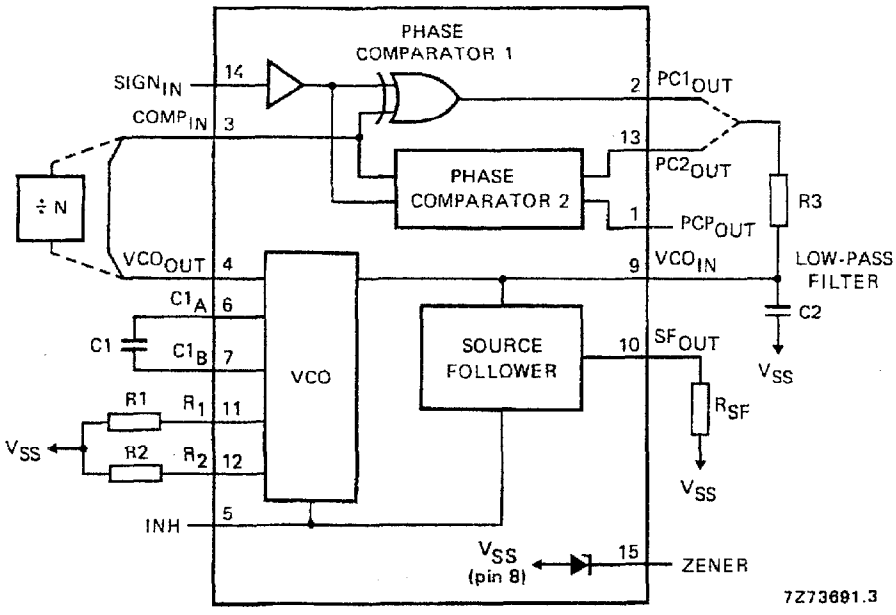


Fig.1 Functional diagram.

HEF4046BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4046BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4046BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

FAMILY DATA

See Family Specifications

I_{DD} LIMITS category MSI

See further on in this data.

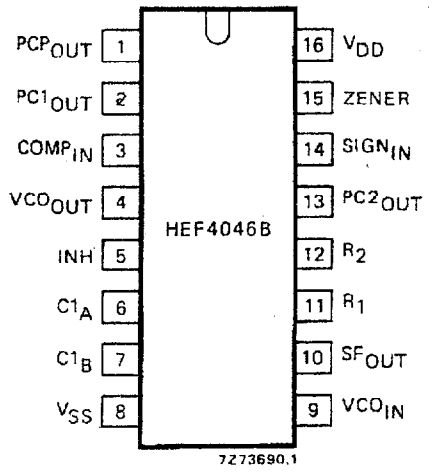


Fig.2 Pinning diagram.

PINNING

1. Phase comparator pulse output
2. Phase comparator 1 output
3. Comparator input
4. VCO output
5. Inhibit input
6. Capacitor C1 connection A
7. Capacitor C1 connection B
8. V_{SS}
9. VCO input
10. Source-follower output
11. Resistor R1 connection
12. Resistor R2 connection
13. Phase comparator 2 output
14. Signal input
15. Zener diode input for regulated supply.

FUNCTIONAL DESCRIPTION

VCO part

The VCO requires one external capacitor (C1) and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency off-set if required. The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at pin 10. If this pin (SF_{OUT}) is used, a load resistor (R_{SF}) should be connected from this pin to V_{SS}; if unused, this pin should be left open. The VCO output (pin 4) can either be connected directly to the comparator input (pin 3) or via a frequency divider. A LOW level at the inhibit input (pin 5) enables the VCO and the source follower, while a HIGH level turns off both to minimize stand-by power consumption.

Phase comparators

The phase-comparator signal input (pin 14) can be direct-coupled, provided the signal swing is between the standard HE4000B family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at the signal input in case of smaller swings. Phase comparator 1 is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50% duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to $\frac{1}{2} V_{DD}$ when there is no signal or noise at the signal input. The average voltage to the VCO input is supplied by the low-pass filter connected to the output of phase comparator 1. This also causes the VCO to oscillate at the centre frequency (f_o). The frequency capture range ($2 f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out of lock. The frequency lock range ($2 f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With phase comparator 1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. Phase comparator 1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal. A typical behaviour of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO centre frequency. Another typical behaviour is, that the phase angle between the signal and comparator input varies between 0° and 180° and is 90° at the centre frequency. Figure 3 shows the typical phase-to-output response characteristic.

Phase comparator 2 is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers having a common output node. When the p-type or n-type drivers are ON, they pull the output up to V_{DD} or down to V_{SS} respectively. This type of phase comparator only acts on the positive-going edges of the signals at $SIGN_{IN}$ and $COMP_{IN}$. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain OFF and thus the phase comparator output becomes an open circuit and keeps the voltage at the capacitor of the low-pass filter constant.

Moreover, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level which can be used for indicating a locked condition. Thus, for phase comparator 2 no phase difference exists between the signal and comparator inputs over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both p and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator 2 . Figure 5 shows typical waveforms for a PLL employing this type of phase comparator in locked condition.

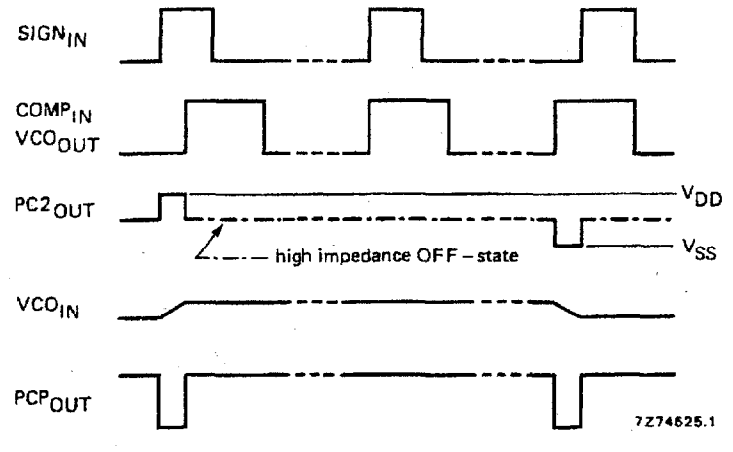


Fig.5 Typical waveforms for phase-locked loop employing phase comparator 2 in locked condition.

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
VCO							
Operating supply voltage		V_{DD}	3		15	V	as fixed oscillator only
			5		15	V	phase-locked loop operation
Power dissipation	5	P		150		µW	f_o = 10 kHz; R1 = 1 MΩ; R2 = ∞; VCO_{IN} at ½ V_{DD}; see also Figs 10 and 11
	10			2500		µW	
	15			9000		µW	
Maximum operating frequency	5	f_{max}	0,5	1,0		MHz	VCO_{IN} at V_{DD}; R1 = 10 kΩ; R2 = ∞; C1 = 50 pF
	10		1,0	2,0		MHz	
	15		1,3	2,7		MHz	
Temperature/ frequency stability	5			0,22—0,30		%/°C	no frequency offset (f_{min} = 0); see also note 1
	10			0,04—0,05		%/°C	
	15			0,01—0,05		%/°C	
	5			0—0,22		%/°C	with frequency offset (f_{min} > 0); see also note 1
	10			0—0,04		%/°C	
	15			0—0,01		%/°C	
Linearity	5			0,50		%	R1 > 10 kΩ — see Fig.13
	10			0,25		%	R1 > 400 kΩ — and Figs 14
	15			0,25		%	R1 = 1 MΩ — 15 and 16
Duty factor at VCO_{OUT}	5	δ		50		%	
	10			50		%	
	15			50		%	
Input resistance at VCO_{IN}	5	R_{IN}		10^6		MΩ	
	10			10^6		MΩ	
	15			10^6		MΩ	
Source follower							
Offset voltage VCO_{IN} minus SF_{OUT}	5			1,7		V	R_{SF} = 10 kΩ; VCO_{IN} at ½ V_{DD}
	10			2,0		V	
	15			2,1		V	
	5			1,5		V	R_{SF} = 50 kΩ; VCO_{IN} at ½ V_{DD}
	10			1,7		V	
	15			1,8		V	
Linearity	5			0,3		%	R_{SF} > 50 kΩ; see Fig.13
	10			1,0		%	
	15			1,3		%	
Zener diode							
Zener voltage		V_Z		7,3		V	I_Z = 50 µA
Dynamic resistance		R_Z		25		Ω	I_Z = 1 mA

Notes

1. Over the recommended component range.

DESIGN INFORMATION

CHARACTERISTIC	USING PHASE COMPARATOR 1	USING PHASE COMPARATOR 2
No signal on $SIGN_{IN}$	VCO in PLL system adjusts to centre frequency (f_o)	VCO in PLL system adjusts to min. frequency (f_{min})
Phase angle between $SIGN_{IN}$ and $COMP_{IN}$	90° at centre frequency (f_o), approaching 0° and 180° at ends of lock range (2 f_L)	always 0° in lock (positive-going edges)
Locks on harmonics of centre frequency	yes	no
Signal input noise rejection	high	low
Lock frequency range (2 f_L)	the frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2 f_L = full VCO frequency range = $f_{max} - f_{min}$	
Capture frequency range (2 f_C)	the frequency range of the input signal on which the loop will lock if it was initially out of lock	
	depends on low-pass filter characteristics; $f_C < f_L$	$f_C = f_L$
Centre frequency (f_o)	the frequency of the VCO when VCO_{IN} at $\frac{1}{2}V_{DD}$	

VCO component selection

Recommended range for R1 and R2: 10 kΩ to 1 MΩ; for C1: 50 pF to any practical value.

1. VCO without frequency offset (R2 = ∞).
   a) Given f_o: use f_o with Fig.7 to determine R1 and C1.
   b) Given f_{max}: calculate f_o from $f_o = \frac{1}{2} f_{max}$; use f_o with Fig.7 to determine R1 and C1.
2. VCO with frequency offset.
   a) Given f_o and f_L : calculate f_{min} from the equation $f_{min} = f_o - f_L$; use f_{min} with Fig.8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$; use $\frac{f_{max}}{f_{min}}$ with Fig. 9 to determine the ratio R2/R1 to obtain R1.
   b) Given f_{min} and f_{max}: use f_{min} with Fig.8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$; use $\frac{f_{max}}{f_{min}}$ with Fig.9 to determine R2/R1 to obtain R1.

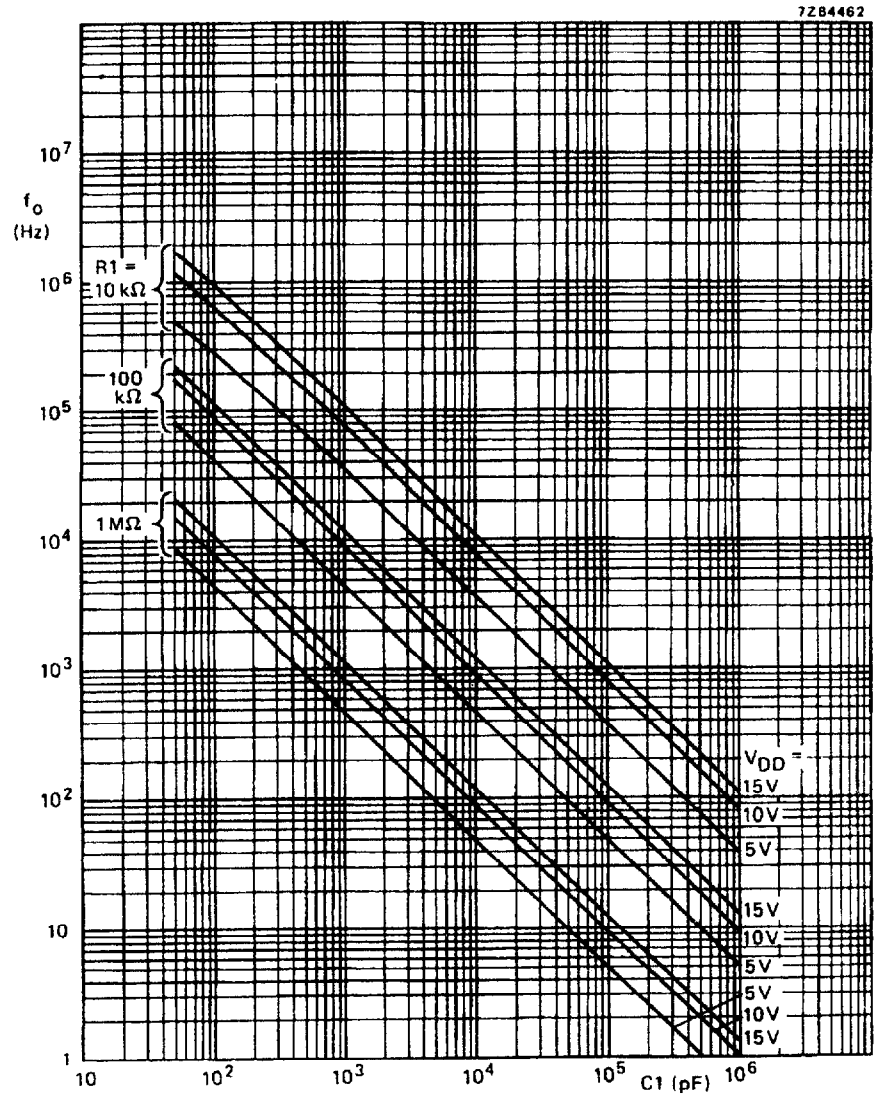


Fig.7 Typical centre frequency as a function of capacitor C1; T_{amb} = 25 °C; VCO_{IN} at ½ V_{DD}; INH at V_{SS}; R_2 = ∞.

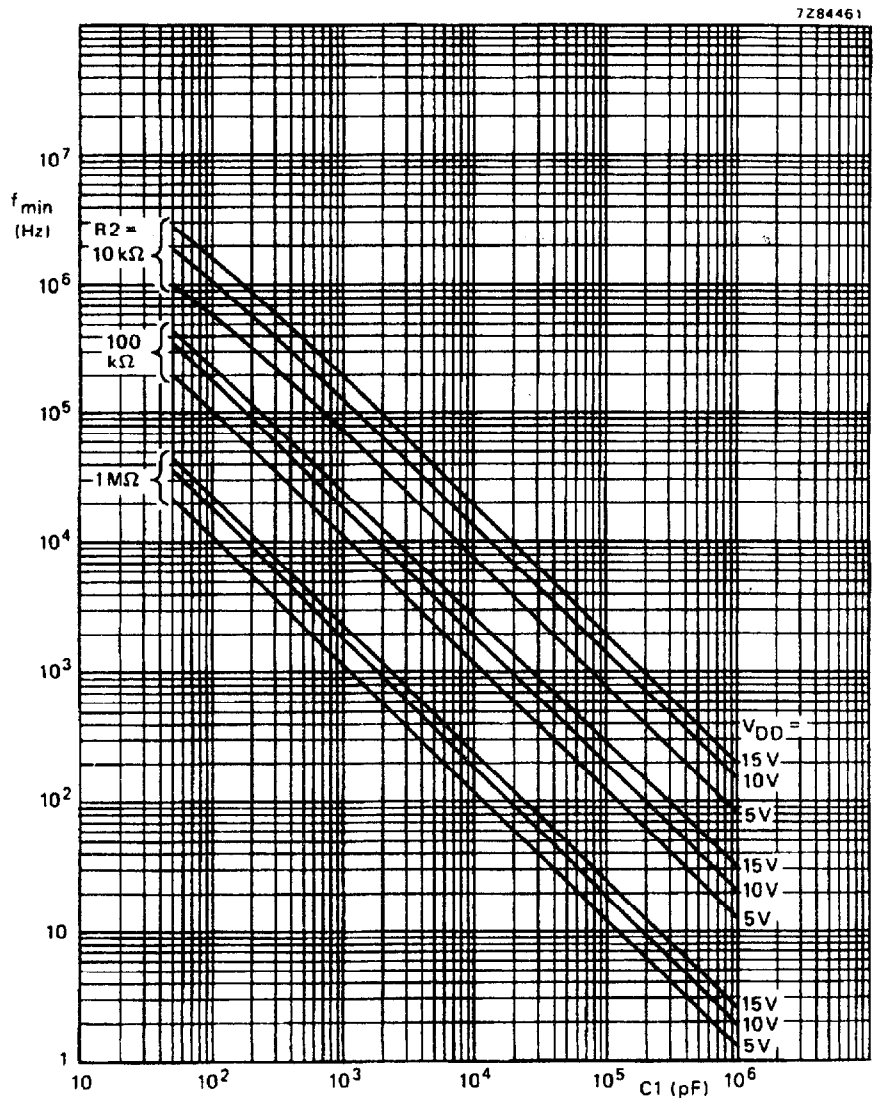


Fig.8 Typical frequency offset as a function of capacitor C1; T_{amb} = 25 °C; VCO_{IN} at V_{SS}; INH at V_{SS}; R1 = ∞.

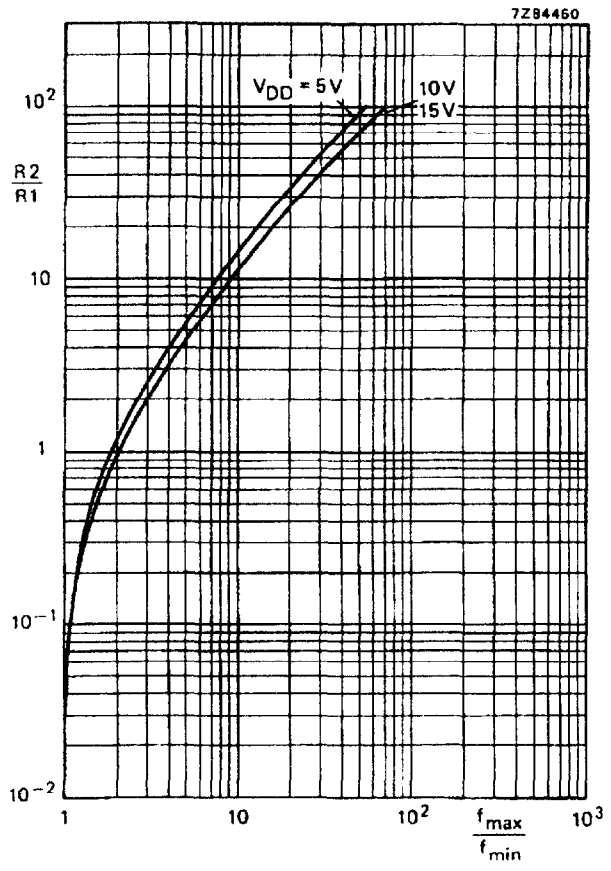


Fig.9 Typical ratio of R2/R1 as a function of the ratio f_{max}/f_{min}.

DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD77C25, 77P25

DIGITAL SIGNAL PROCESSOR

The μPD77C25, 77P25 are 16-bit fixed point CMOS signal processors intended for real-time digital processing of speech signals.

Each device consists of a parallel multiplier (16 x 16 bits → 31 bits), an ALU (16 bits), an instruction ROM (2,048 x 24 bits), a data ROM (1,024 x 16 bits), a data RAM (256 x 16 bits), I/O ports, and others. All instructions consist of 24 bits or one word instruction are executed in 122 ns (at f_{CLK} = 8.192 MHz) including sum of product computations.

Since signals that interfaces with the host CPU are provided, the μPD77C25, 77P25 can cover a variety of applications, serving as an I/O processor. Moreover, they can also be used as single-chip CPU.

The μPD77C25, 77P25 provide an instruction ROM each four times larger than that of the former product μPD7720 signal processor. Additionally, each device has a data ROM and a data RAM, both of which are two times larger, and a processing speed faster. Furthermore, the μPD77C25, 77P25 can replace the μPD7720 as they have the same pin connections.

The instruction sets of the μPD77C25, 77P25 are upward-compatible with that of the μPD7720 at the assembler source program level.

The μPD77C25 is version with on-chip resources including the instruction ROM and data ROM are constructed in mask ROMs; the μPD77P25 has PROMs. The μPD77P25D is an UVEPROM type and the μPD77P25C/L/GW is an one time PROM (OTP) type.

Remark In this document, the μPD77C25 refers to the μPD77C25, 77P25 unless otherwise specified.

FEATURES

- Biquad Digital Filter (with sampling performed at 8 kHz) : Equivalent to 113 filters
- On-chip exclusive parallel multiplier : 16 bits x 16 bits → 31 bits
- Instruction ROM : 2,048 words x 24 bits
- Data ROM : 1,024 words x 16 bits
- Data RAM : 256 words x 16 bits
- Dual accumulator method
- On-chip serial input and serial output interfaces
- On-chip host CPU bus interface
- On-chip DMA interface
- Upward-compatible with the μPD7720 at assembler source program level
- Pin-compatible with μPD7720
- Low-power CMOS

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Date Published June 1997 N
Printed in Japan

The mark ★ shows major revised points.

HOLT INC.
INTEGRATED CIRCUITS

HI-8382, HI-8383

February 2003

ARINC 429 DIFFERENTIAL LINE DRIVER

GENERAL DESCRIPTION

The HI-8382 and HI-8383 bus interface products are silicon gate CMOS devices designed as a line driver in accordance with the ARINC 429 bus specifications.

Inputs are provided for clocking and synchronization. These signals are ANDd with the DATA inputs to enhance system performance and allow the HI-8382 to be used in a variety of applications. Both logic and synchronization inputs feature built-in 2,000V minimum ESD input protection as well as TTL and CMOS compatibility.

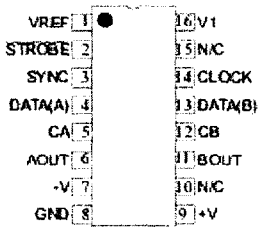
The differential outputs of the HI-8382 are independently programmable to either the high speed or low speed ARINC 429 output rise and fall time specifications through the use of two external capacitors. The output voltage swing is also adjustable by the application of an external voltage to the VREF input. The HI-8382 has on-chip Zener diodes in series with a fuse to each differential output protecting the ARINC bus from an overvoltage failure. The outputs each have a series resistance of 37.5 ohms. The HI-8383 is identical to the HI-8382 except that the series resistors are 13 ohms and the overvoltage protection circuitry has been eliminated.

The updated HI-318X and HI-8585 ARINC 429 line drivers are recommended for all new designs where logic signals must be converted to ARINC 429 levels such as a user ASIC, the HI-3282 or HI-8282A ARINC 429 Serial Transmitter/Dual Receiver, the HI-6010 ARINC 429 Transmitter/Receiver or the HI-8783 ARINC interface device. Holt products are readily available for both industrial and military applications. Please contact the Holt Sales Department for additional information, including data sheets for any of the Holt products mentioned above.

FEATURES

- Low power CMOS
- TTL and CMOS compatible inputs
- Programmable output voltage swing
- Adjustable ARINC rise and fall times
- Operates at data rates up to 100 Kbits
- Overvoltage protection
- Industrial and Military temperature ranges
- DSCC SMD part number

PIN CONFIGURATION (Top View)

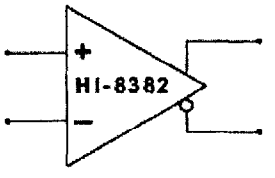


HI-8382C / CT / CM-01 / CM-03
SMD # 5962-8687901EA

16 - PIN CERAMIC SIDE-BRAZED DIP

(See Page 6 for additional package pin configurations)

FUNCTION



ARINC 429 DIFFERENTIAL LINE DRIVER

TRUTH TABLE

SYNC	CLOCK	DATA(A)	DATA(B)	AOUT	BOUT	COMMENTS
X	L	X	X	0V	0V	NULL
L	X	X	X	0V	0V	NULL
H	H	L	L	0V	0V	NULL
H	H	L	H	-VREF	+VREF	LOW
H	H	H	L	+VREF	-VREF	HIGH
H	H	H	H	0V	0V	NULL

FUNCTIONAL DESCRIPTION

The SYNC and CLOCK inputs establish data synchronization utilizing two AND gates, one for each data input. Each logic input, including the power enable (STROBE) input, are TTL/CMOS compatible. Besides reducing chip current drain, STROBE also floats each output. However the overvoltage fuses and diodes of the HI-8382 are not switched out.

Figure 1 illustrates a typical ARINC 429 bus application. Three power supplies are necessary to operate the HI-8382; typically +15V, -15V and +5V. The chip also works with ±12V supplies. The +5V supply can also provide a reference voltage that determines the output voltage swing. The differential output voltage swing will equal $2V_{REF}$. If a value of V_{REF} other than +5V is needed, a separate +5V power supply is required for pin V1.

With the DATA (A) input at a logic high and DATA (B) input at a logic low, AOUT will switch to the $+V_{REF}$ rail and BOUT will switch to the $-V_{REF}$ rail (ARINC HIGH state). With both data input signals at a logic low state, the outputs will both switch to 0V (ARINC NULL state).

The driver output impedance, ROUT, is nominally 75 ohms. The rise and fall times of the outputs can be calibrated through the selection of two external capacitor values that are connected to the CA and CB input pins. Typical values for high-speed operation (100KBPS) are CA = CB = 75pF and for low-speed operation (12.5 to 14KBPS) CA = CB = 500pF. The driver can be externally powered down by applying a logic high to the STROBE input pin. If this feature is not being used, the pin should be tied to ground.

The CA and CB pins are inputs to unity gain amplifiers. Therefore they must be allowed to swing to -5V. Provision to switch capacitors must be done with analog switches that allow voltages below the ground.

Both ARINC outputs of the HI-8382 are protected by internal fuses capable of sinking between 800 - 900 mA for short periods of time (125µs).

POWER SUPPLY SEQUENCING

The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is +V followed by V1, always ensuring that +V is the most positive supply. The -V supply is not critical and can be asserted at any time.

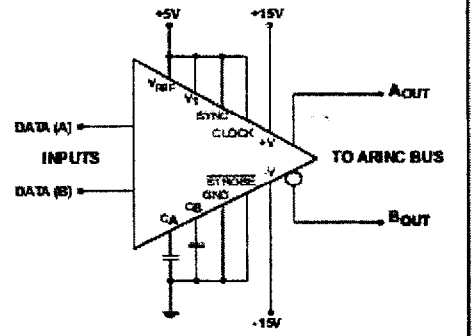


Figure 1. ARINC 429 BUS APPLICATION

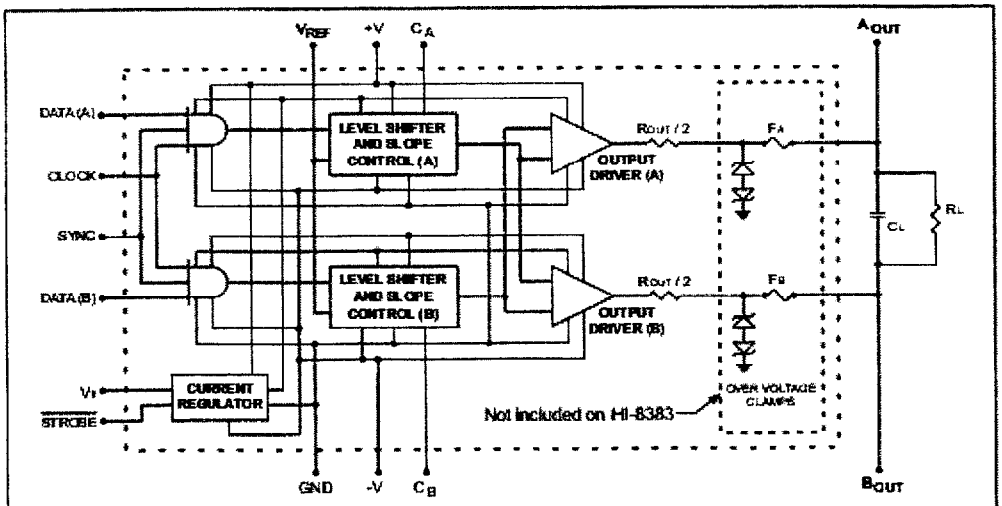


Figure 2. FUNCTIONAL BLOCK DIAGRAM

TABLE 3. DD-03282 SPECIFICATION
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	DATA RATE 100 kb/s MIN	DATA RATE 100 kb/s MAX	DATA RATE 12.5 kb/s MIN	DATA RATE 12.5 kb/s MAX	UNITS
CK_{DC}	1MCK Duty Cycle	40	60	40	60	%
T_{CRF}	1MCK Rise/Fall Time		10		10	ns
T_{MR}	Master Reset Pulse Width	200		200		ns
T_{DR}	Transmitter Data Rate (1MCK = 1 MHz)	99	101	12.4	12.6	kbps
R_{DR}	Receiver Data Rate (1MCK = 1 MHz)	95	105	9.0	14.5	kbps

GENERAL DESCRIPTION

ARINC 429, as defined and described in ARINC Specification 429 Digital Information Transfer System, Mark 33, has been in use since 1977. It is the foundation for digital communications in modern civil aircraft. Certification issues have driven 429 to be defined as a simplex bus (one transmitter, multiple receivers) for point-to-point communications using 32-bit words with odd parity and 12-14.5 kHz (Lo Speed) or 100 kHz (Hi Speed) operation.

The DD-03282 provides an interface between a standard avionics type serial digital data bus and most typical 16-bit-wide microcomputer data buses. The avionics buses supported by this device include:

ARINC 429

ARINC 571

ARINC 575

ARINC 706

Delco IRS 9600 Baud Data Bus

ARINC 561 (with support circuitry)

The interface circuit consists of a transmitter circuit, two identical, but independent receiver circuits, and a user-programmable control register for use in selecting operating options. The transmitter circuit contains an 8 word x 32 bit buffer and control logic which allows the user to write a block of data into the transmitter. Once the user enables the transmitter, the data block is automatically sent without further attention.

Two receiver circuits each operate identically. Each contains a line receiver which provides a direct electrical interface to an ARINC-429 data bus. Incoming data is shifted into a 32-bit shift register and latched into a data buffer if a valid word is received. The control register allows the user to select the various options. These include:

Word length (32 or 25 bits).

Transmitter Bit 32 (parity or data).

Transmitter parity (even or odd).

Wraparound self test.

Source/Destination code filtering of received data.

Transmitter data rate (Hi Speed or Lo Speed).

Receiver data rate (Hi Speed or Lo Speed).

The Transceiver fully supports the ARINC 429 data rates and receiver electrical characteristics over temperature (-55° C to +125° C) and voltages (4.5 VDC to 5.5 VDC). It interfaces with TTL, CMOS, or NMOS support circuitry using a standard 5 volt Vcc supply.

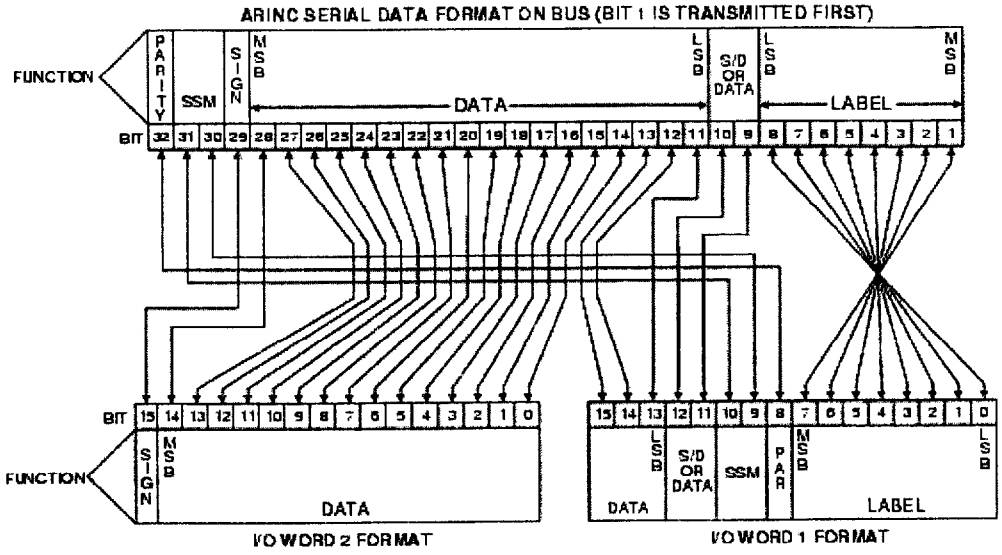


FIGURE 3. MAPPING OF SERIAL DATA TO/FROM WORD 1 AND WORD 2 — 32-BIT FORMAT

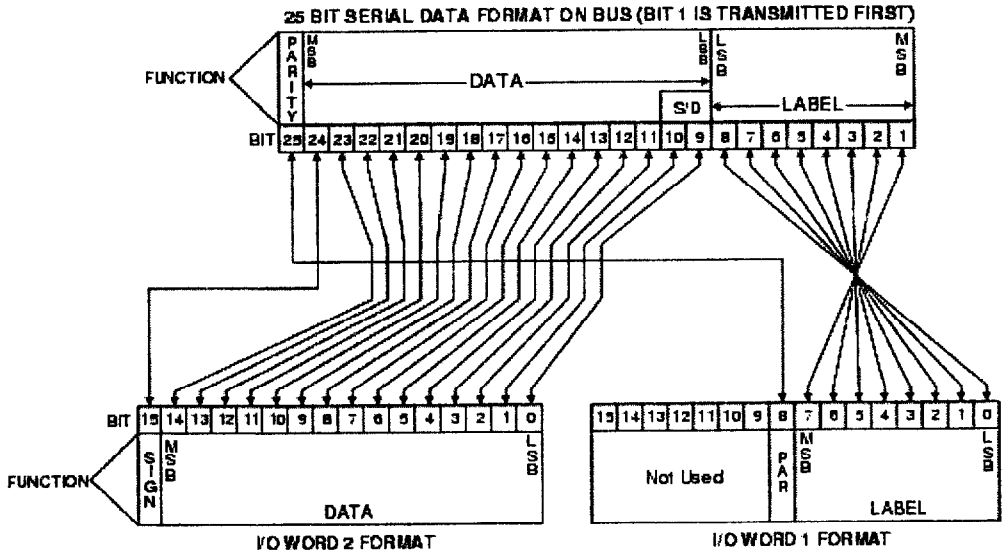


FIGURE 4. MAPPING OF SERIAL DATA TO/FROM WORD 1 AND WORD 2 — 25-BIT FORMAT

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