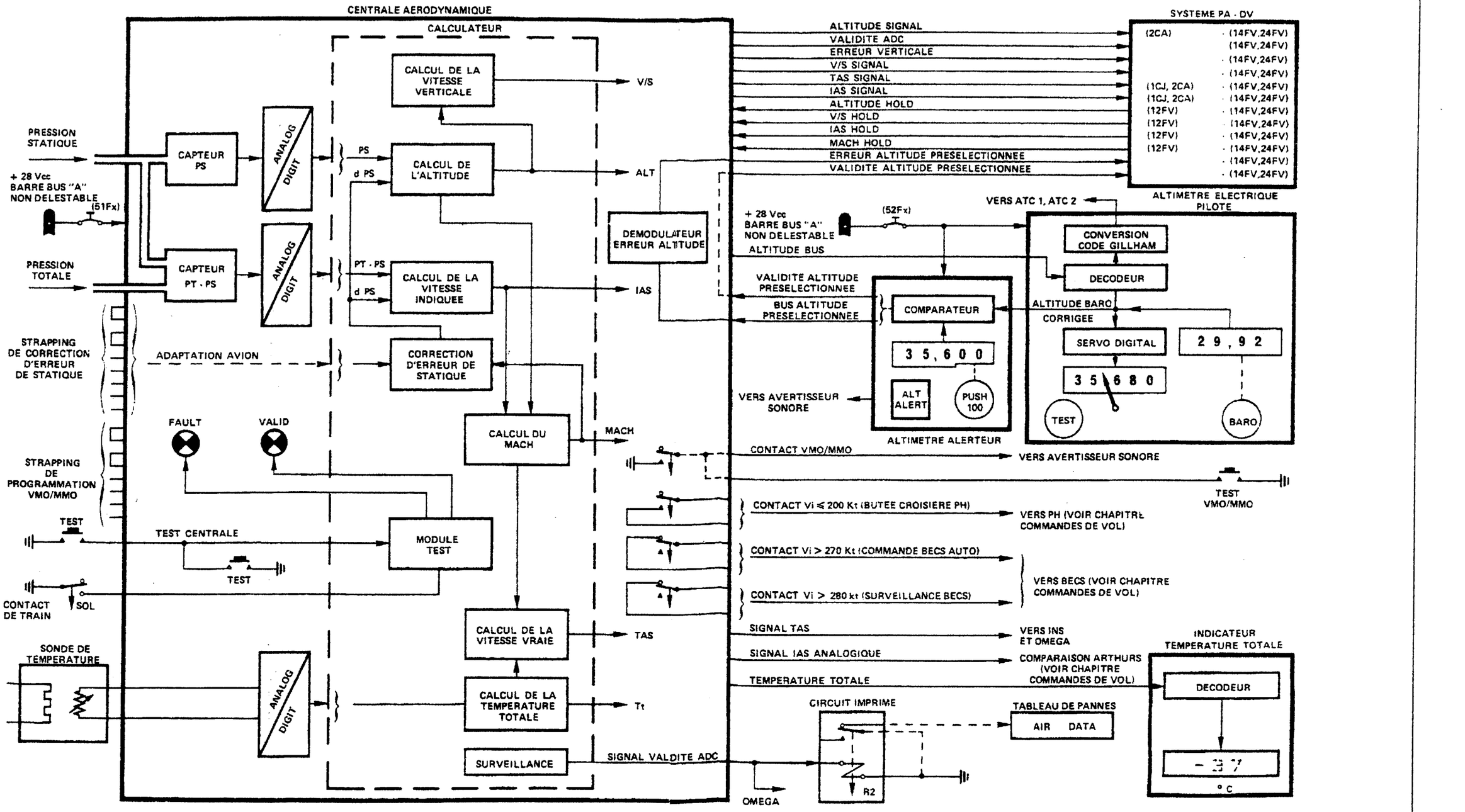
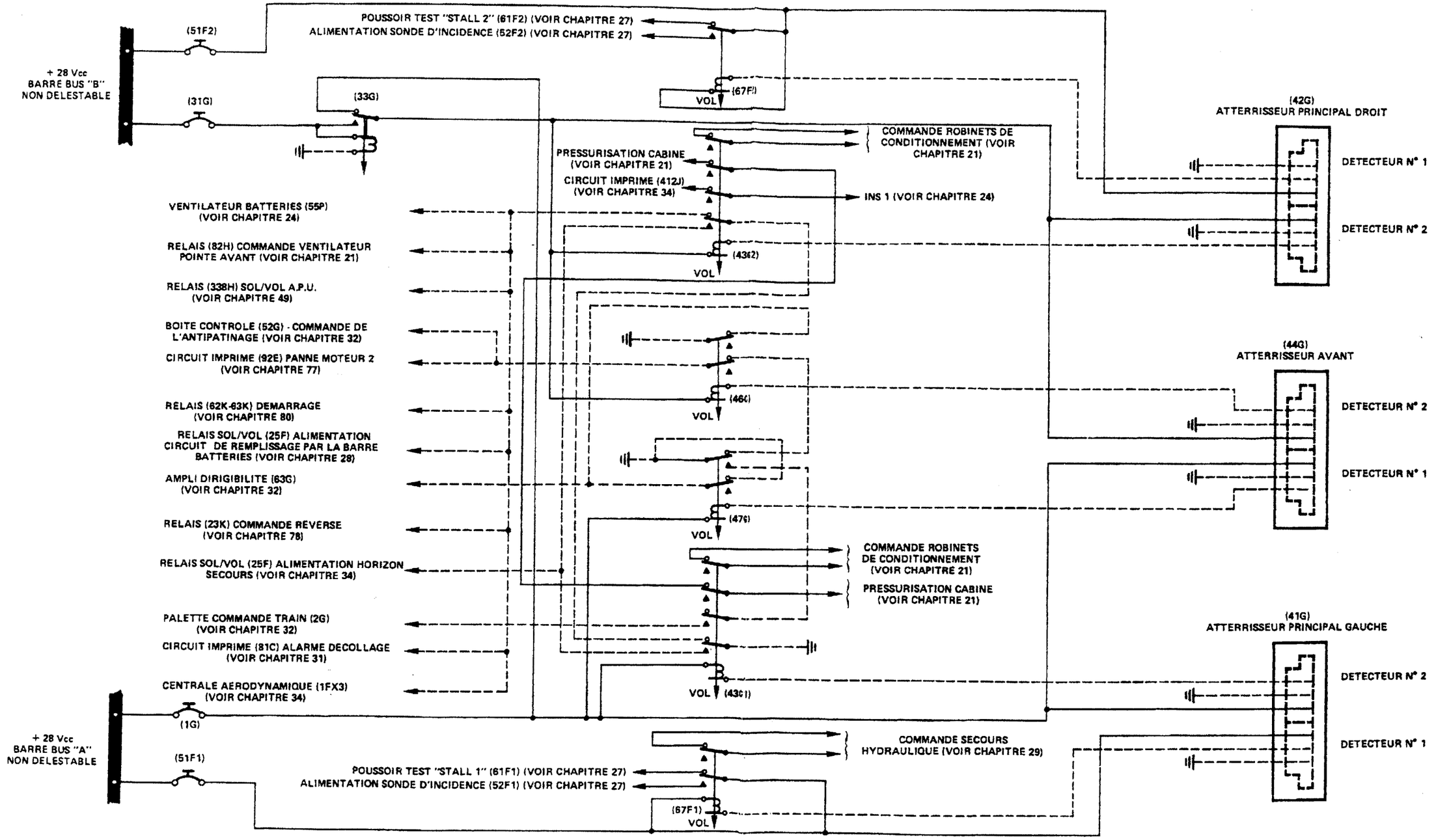
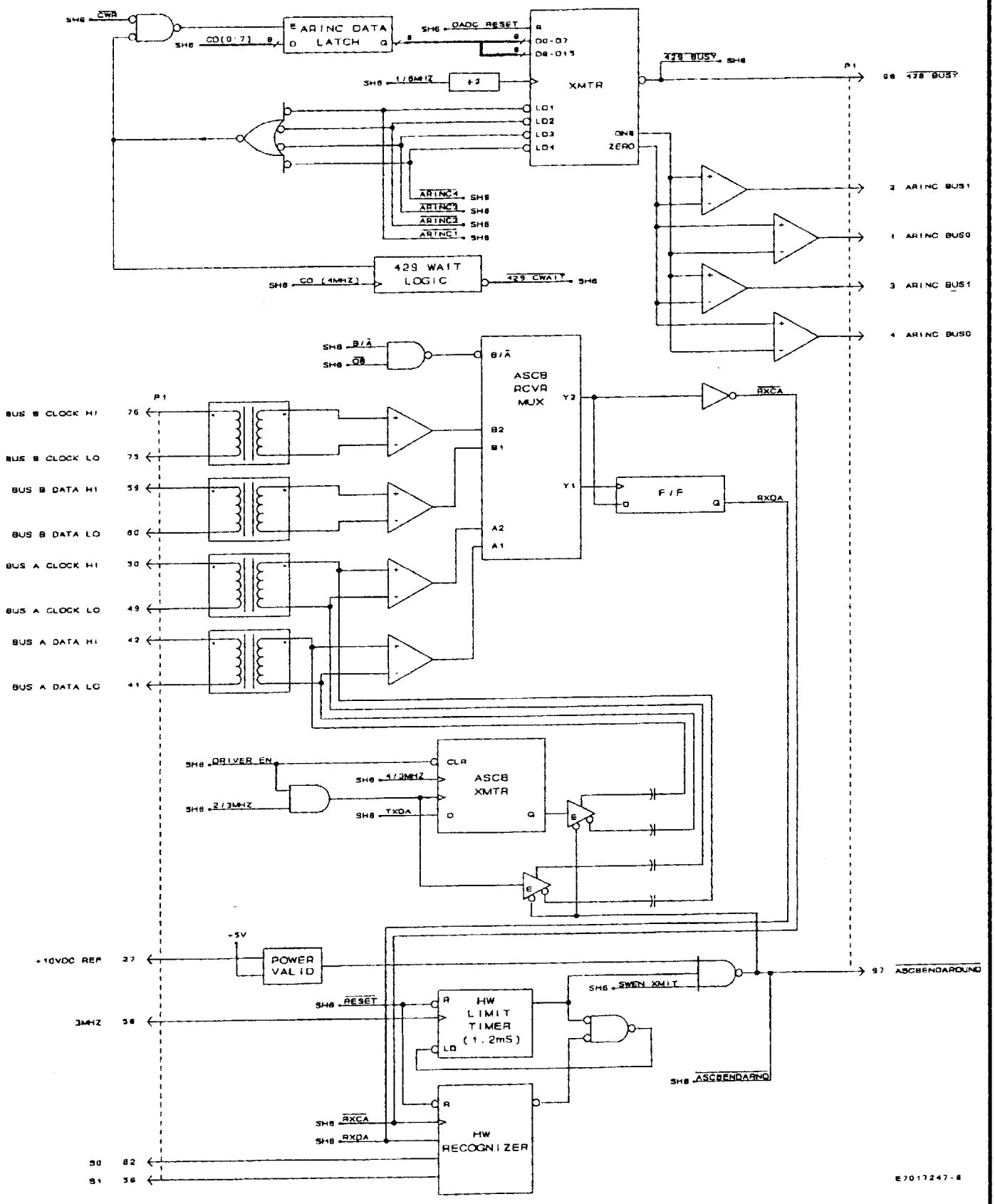


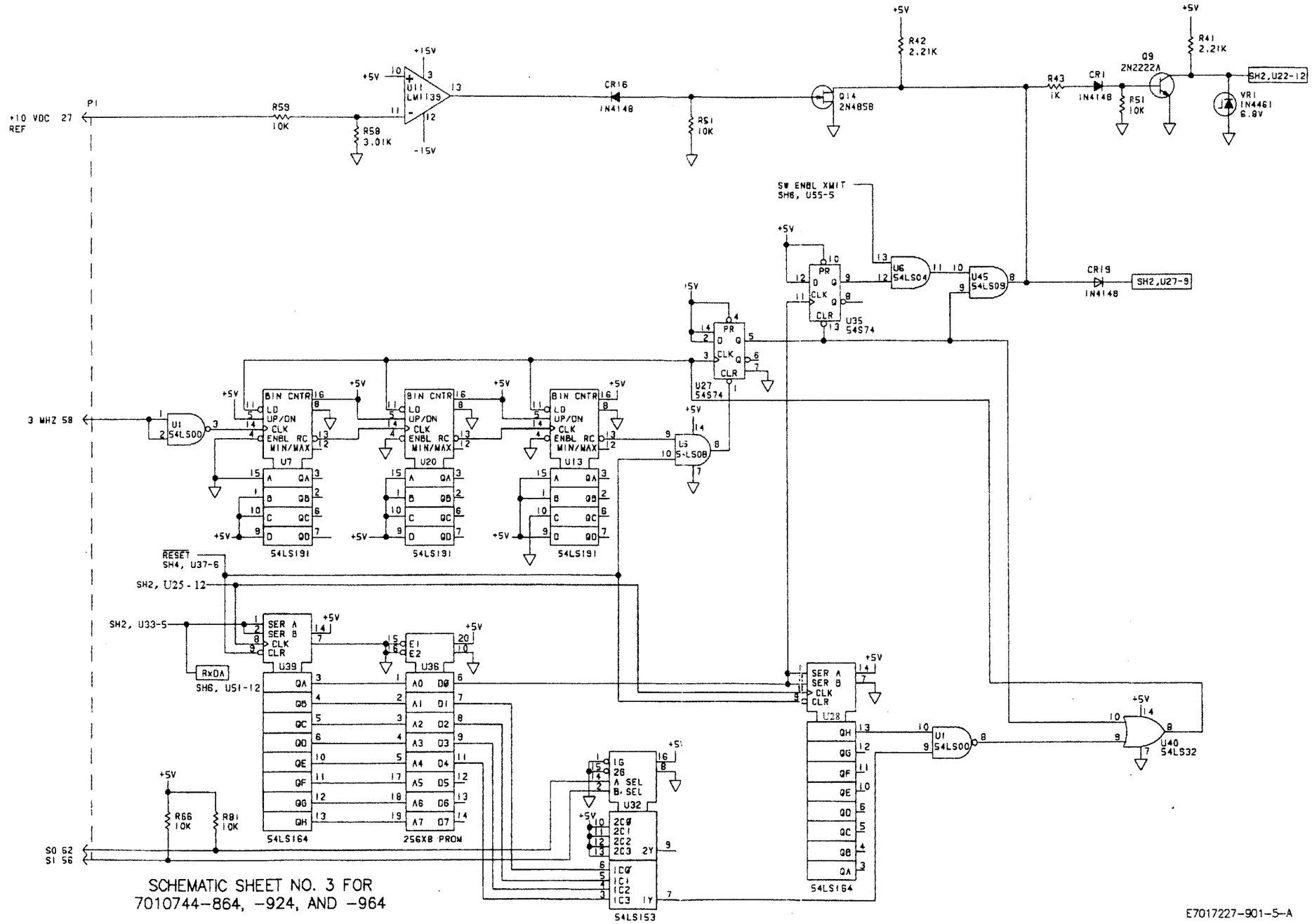
Centrale aérodynamique - Schéma de principe



Détection sol-vol - Schéma de principe

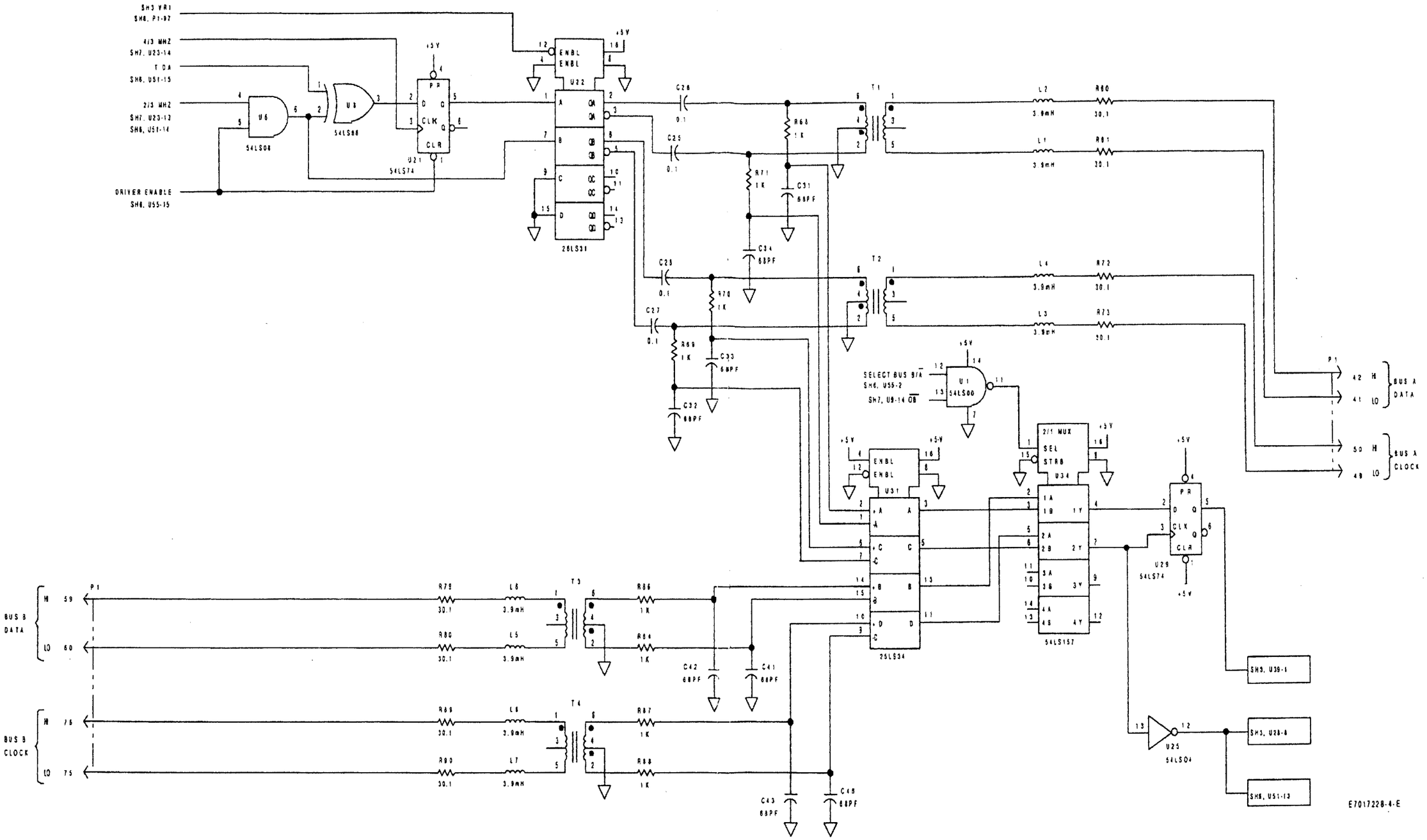


BACALAUREAT PROFESSIONNEL AERONAUTIQUE
Option Avionique
Epreuve E1A : Etude d'un système d'un aéronef
DUREE : 4 heures COEFFICIENT : 2
DOSSIER TECHNIQUE Page DT 17 / 29



SCHEMATIC SHEET NO. 3 FOR
7010744-864, -924, AND -964

ARINC/ASCB Circuit Card Assembly - A3
Figure 111 (Sheet 3)



SCHEMATIC DIAGRAM SHEET NO. 2

ARINC 429/ASCB Circuit Card Assembly - A3
(Sheet 2)

TYPES SN5408, SN54LS08, SN54S08, SN7408, SN74LS08, SN74S08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

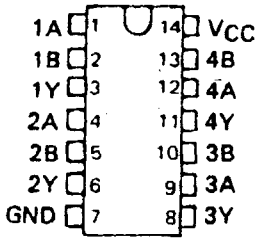
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic diagram (each gate)

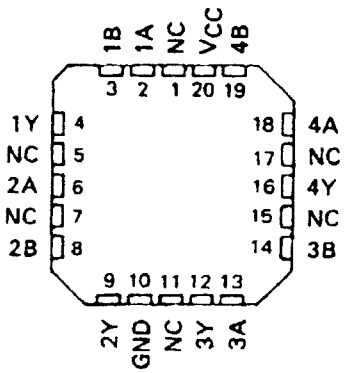
positive logic

$$Y = A \cdot B \text{ or } Y = \overline{\overline{A} + \overline{B}}$$

SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
SN7408 . . . J OR N PACKAGE
SN74LS08, SN74S08 . . . D, J OR N PACKAGE
(TOP VIEW)



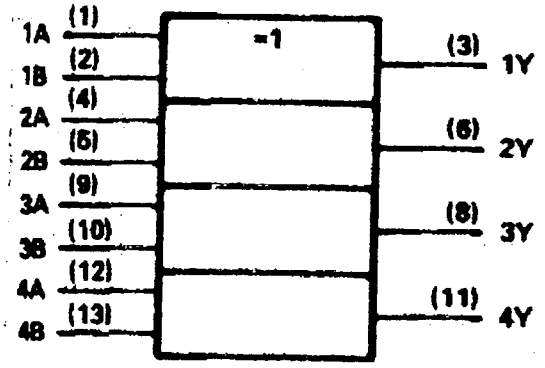
SN54LS08, SN54S08 . . . FK PACKAGE
SN74LS08, SN74S08
(TOP VIEW)



NC - No internal connection

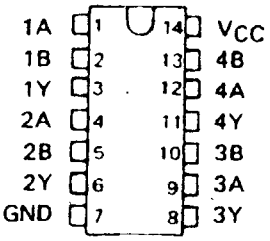
schematics of inputs and outputs

logic symbol

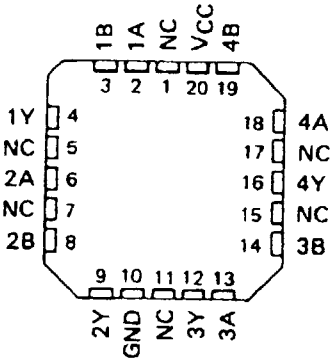


Pin numbers shown are for J and N packages.

SN5486, SN54LS86A, SN54S86 . . . J OR W PACKAGE
SN7486 . . . J OR N PACKAGE
SN74LS86A, SN74S86 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS86A, SN54S86 . . . FK PACKAGE
SN74LS86A, SN74S86
(TOP VIEW)



NC - No internal connection

FUNCTION TABLES

TYPE	INPUTS A	INPUTS B	OUTPUT Y
'86, 'LS86A, 'S86	L	L	L
	L	H	H
	H	L	H
	H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'LS86A	10 ns	30.5 mW
'S86	7 ns	250 mW

TYPES SN5474, SN54LS74A, SN54S74
SN7474, SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

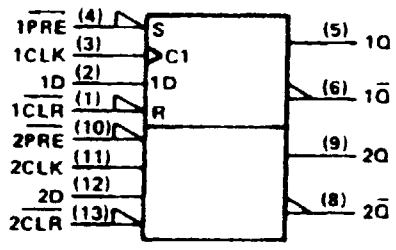
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

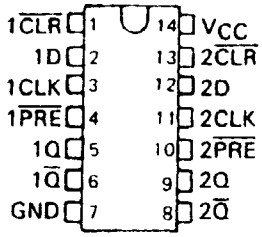
† The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol

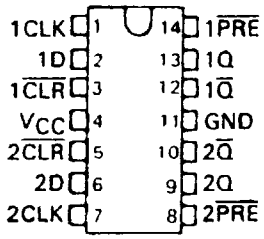


Pin numbers shown on logic notation are for D, J or N packages.

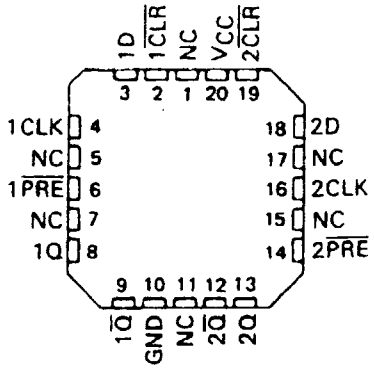
SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . J OR N PACKAGE
SN74LS74A, SN74S74 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

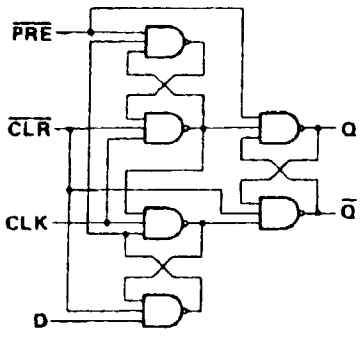


SN54LS74A, SN54S74 . . . FK PACKAGE
SN74LS74A, SN74S74
(TOP VIEW)



NC – No internal connection

logic diagram



TYPES SN5404, SN54LS04, SN54S04
SN7404, SN74LS04, SN74S04
HEX INVERTERS

REVISED DECEMBER 1983

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

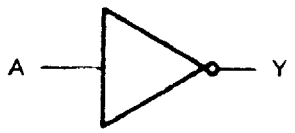
These devices contain six independent inverters.

The SN5404, SN54LS04 and SN54S04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7404, SN74LS04 and SN74S04 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

INPUTS A	OUTPUT Y
H	L
L	H

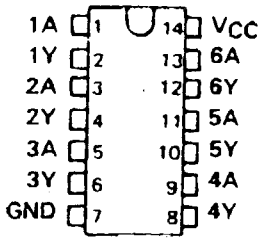
logic diagram (each inverter)



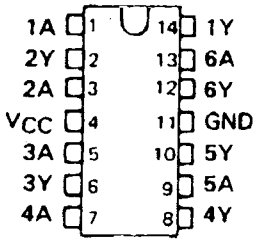
positive logic

$$Y = \overline{A}$$

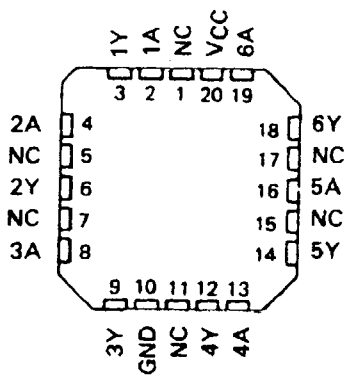
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR PACKAGE
SN7404 . . . J OR N PACKAGE
SN74LS04, SN74S04 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
SN74LS04, SN74S04
(TOP VIEW)



NC - No internal connection

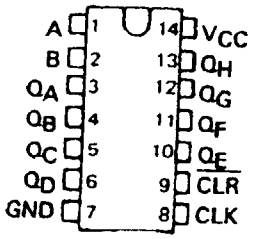
TYPES SN54164, SN74LS164, SN74164, SN74LS164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

MARCH 1974—REVISED DECEMBER 1983

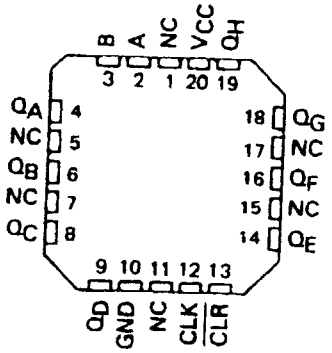
- **Gated Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Asynchronous Clear**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'164	36 MHz	21 mW per bit
'LS164	36 MHz	10 mW per bit

SN54164, SN54LS164 . . . J OR W PACKAGE
SN74164 . . . J OR N PACKAGE
SN74LS164 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS164 . . . FK PACKAGE
SN74LS164
(TOP VIEW)



NC — No internal connection

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74164 and SN74LS164 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

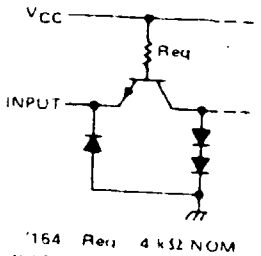
INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

schematics of inputs and outputs

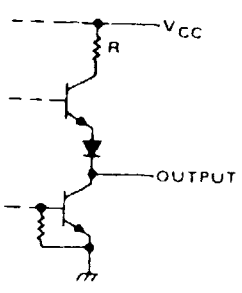
'164

EQUIVALENT OF EACH INPUT



'164 Req 4 kΩ NOM
'L164 Req 8 kΩ NOM

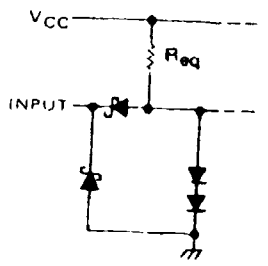
TYPICAL OF ALL OUTPUTS



'164, R 200 Ω NOM

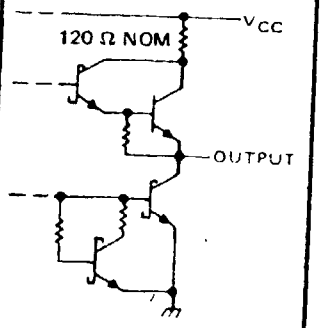
'LS164

EQUIVALENT OF EACH INPUT

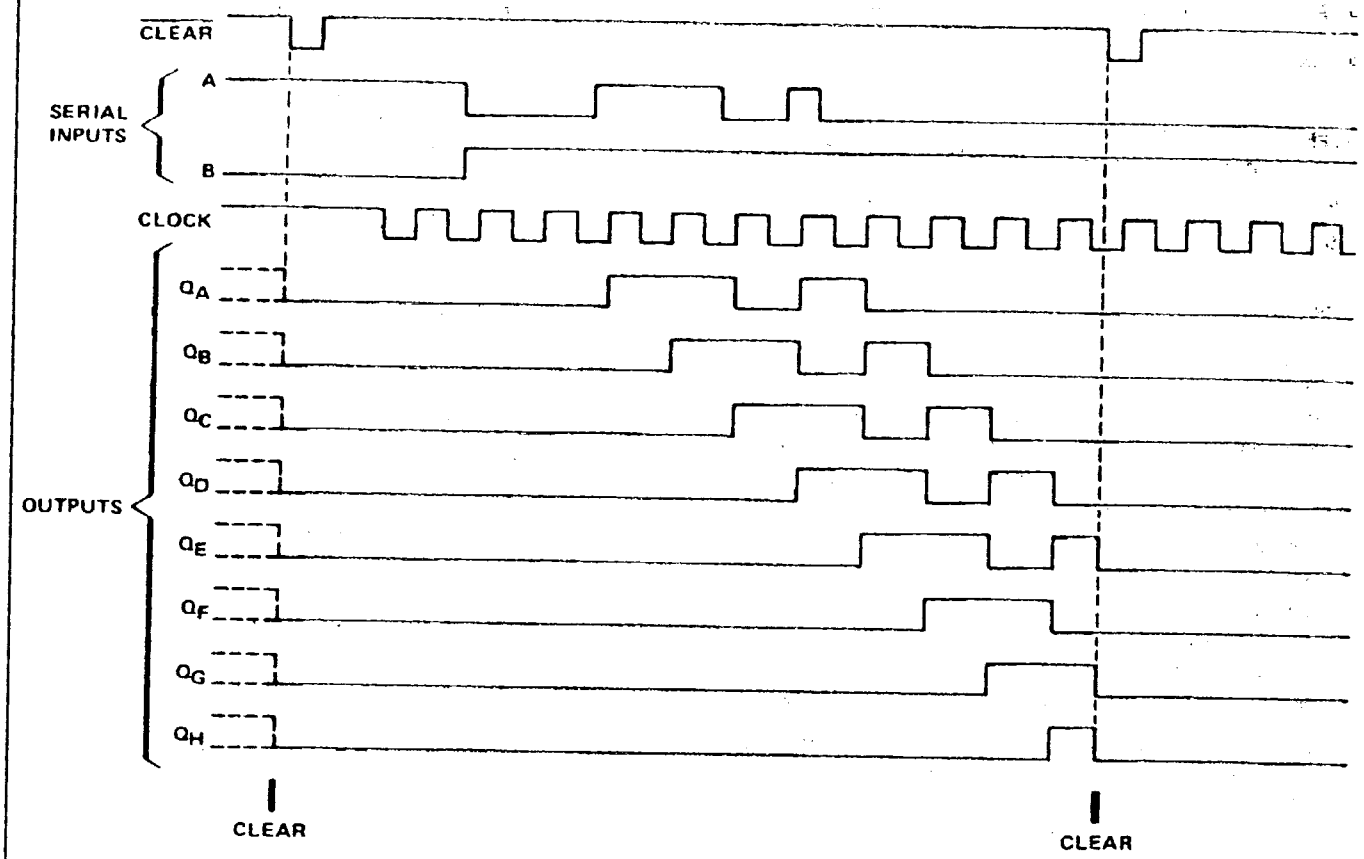


Clear, clock: 17 kΩ NOM
Serial in: 25 kΩ NOM

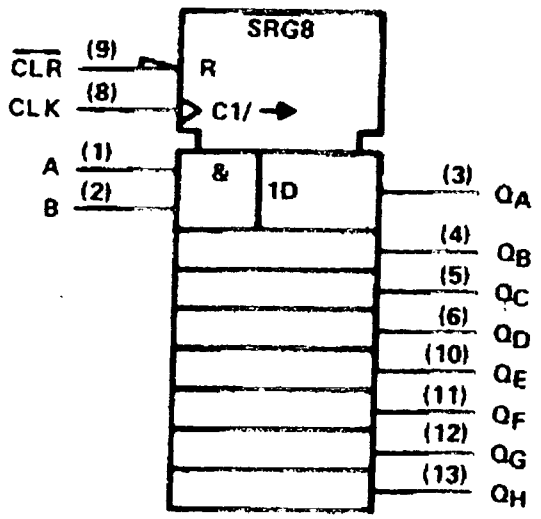
TYPICAL OF ALL OUTPUTS



typical clear, shift, and clear sequences



logic symbol



MOS
LSI

TMS2716
2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

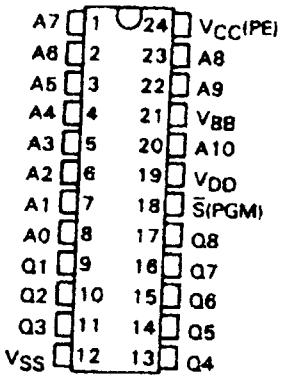
DECEMBER 1979 – REVISED OCTOBER 1983

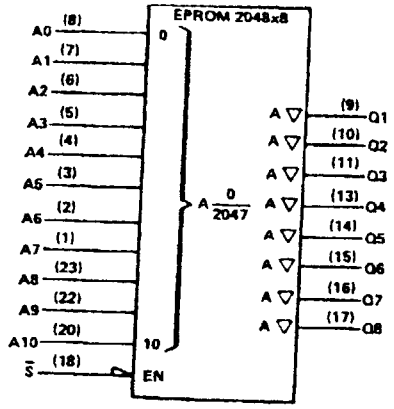
- 2048 X 8 Organization
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Performance Ranges:

	ACCESS TIME (MAX)	CYCLE TIME (MIN)
TMS2716-30	300 ns	300 ns
TMS2716-45	450 ns	450 ns

- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Low Power . . . 315 mW (Typical)

TMS2716 . . . JL PACKAGE
(TOP VIEW)





PIN NOMENCLATURE	
A0-A10	Addresses
Q1-Q8	Data Out
$\overline{S}$(PGM)	Chip Select (Program)
V_{BB}	−5-V Supply
V_{CC}(PE)	+5-V Supply (Program Enable)
V_{DD}	+12-V Supply
V_{SS}	0 V Ground

description

The TMS2716 is an ultra-violet light-erasable, electrically programmable read-only memory. It has 16,384 bits organized as 2048 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 circuits without the use of external pull-up resistors and each output can drive one Series 74 or 74LS TTL circuit without external resistors. The TMS2716 guarantees 250 mV dc noise immunity in the low state. Data outputs are three-state for OR-tying multiple devices on a common bus. The TMS2716 is plug-in compatible with the TMS2708 and the TMS27L08. Pin compatible mask programmed ROMs are available for large volume requirements.

This EPROM is designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. It is supplied in a 24-pin dual-in-line cerpak (JL suffix) package designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers. It is designed for operation from 0 °C to 70 °C.

operation (read mode)

address (A0-A10)

The address-valid interval determines the device cycle time. The 11-bit positive-logic address is decoded on-chip to select one of 2048 words of 8-bit length in the memory array. A0 is the least-significant bit and A10 most-significant bit of the word address.

chip select, program [$\overline{S}$ (PGM)]

When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high, all eight outputs are in a high-impedance state.

program

In the program mode, the chip select feature does not function as pin 18 inputs only the program pulse. The program mode is selected by the V_{CC}(PE) pin. Either 0 V or +12 V on this pin will cause the TMS2716 to assume program cycle.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

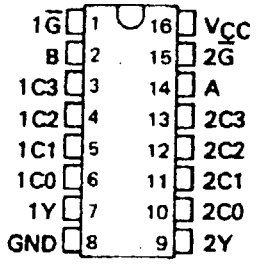
TYPES SN54153, SN54LS153, SN54S153
SN74153, SN74LS153, SN74S153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

DECEMBER 1972–REVISED DECEMBER 1983

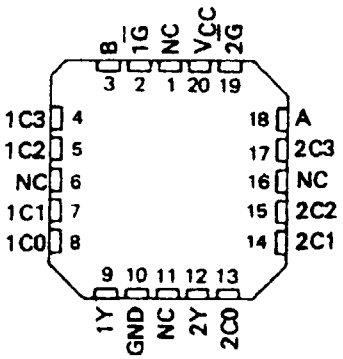
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES			TYPICAL POWER DISSIPATION
	FROM DATA	FROM STROBE	FROM SELECT	
'153	14 ns	17 ns	22 ns	180 mW
'LS153	14 ns	19 ns	22 ns	31 mW
'S153	6 ns	9.5 ns	12 ns	225 mW

SN54153, SN54LS153, SN54S153 . . . J OR W PACKAGE
SN74153 . . . J OR N PACKAGE
SN74LS153, SN74S153 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS153, SN54S153 . . . FK PACKAGE
SN74LS153, SN74S153
(TOP VIEW)



NC - No internal connection

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

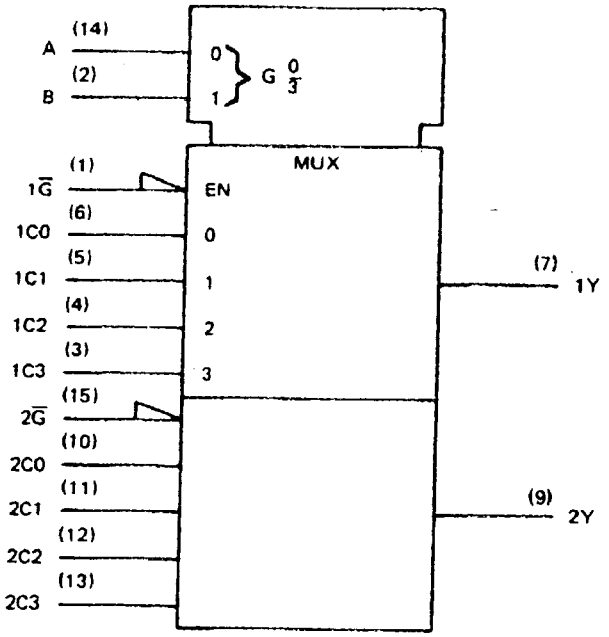
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage : '153, 'S153 . . . . . 5.5 V
'LS153 . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

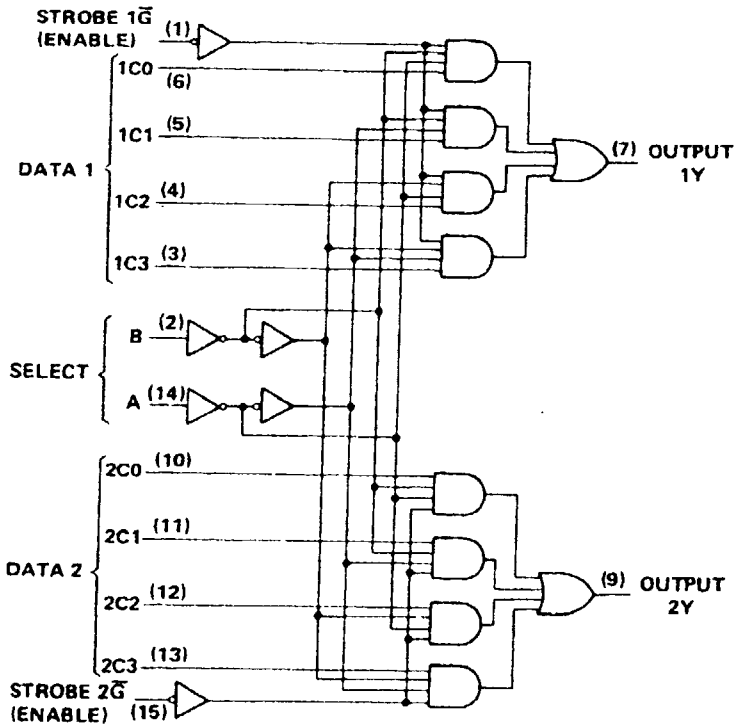
NOTE 1: Voltage values are with respect to network ground terminal.

TYPES SN54153, SN54LS153, SN54S153
SN74153, SN74LS153, SN74S153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

logic symbol



logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

GLOSSAIRE

ARTHUR	:	**ART**iculation **H**ydraulique à **U**nité **R**églable : Systèmes de limitation des commandes gauchissement et profondeur
Contacteur de Vi	:	Manocontact
Alt	:	Altitude
Δp	:	Variation de pression
TAT	:	Total Air Temperature
TAS	:	True Air Speed
SAT	:	Static Air Temperature
IAS	:	Indicated Air Speed
INS	:	Inertial Navigation System
EFIS	:	Electronic Flight Instrument System
PH	:	Plan Horizontal
VMO	:	Vitesse Maxi Opérationnelle
MMO	:	Mach Maxi Opérationnel

FORMULAIRE

$$P_d = \frac{(\rho \times V^2)}{2} = \frac{1}{2}\rho \times V^2$$

$$P_d = P_T - P_S$$