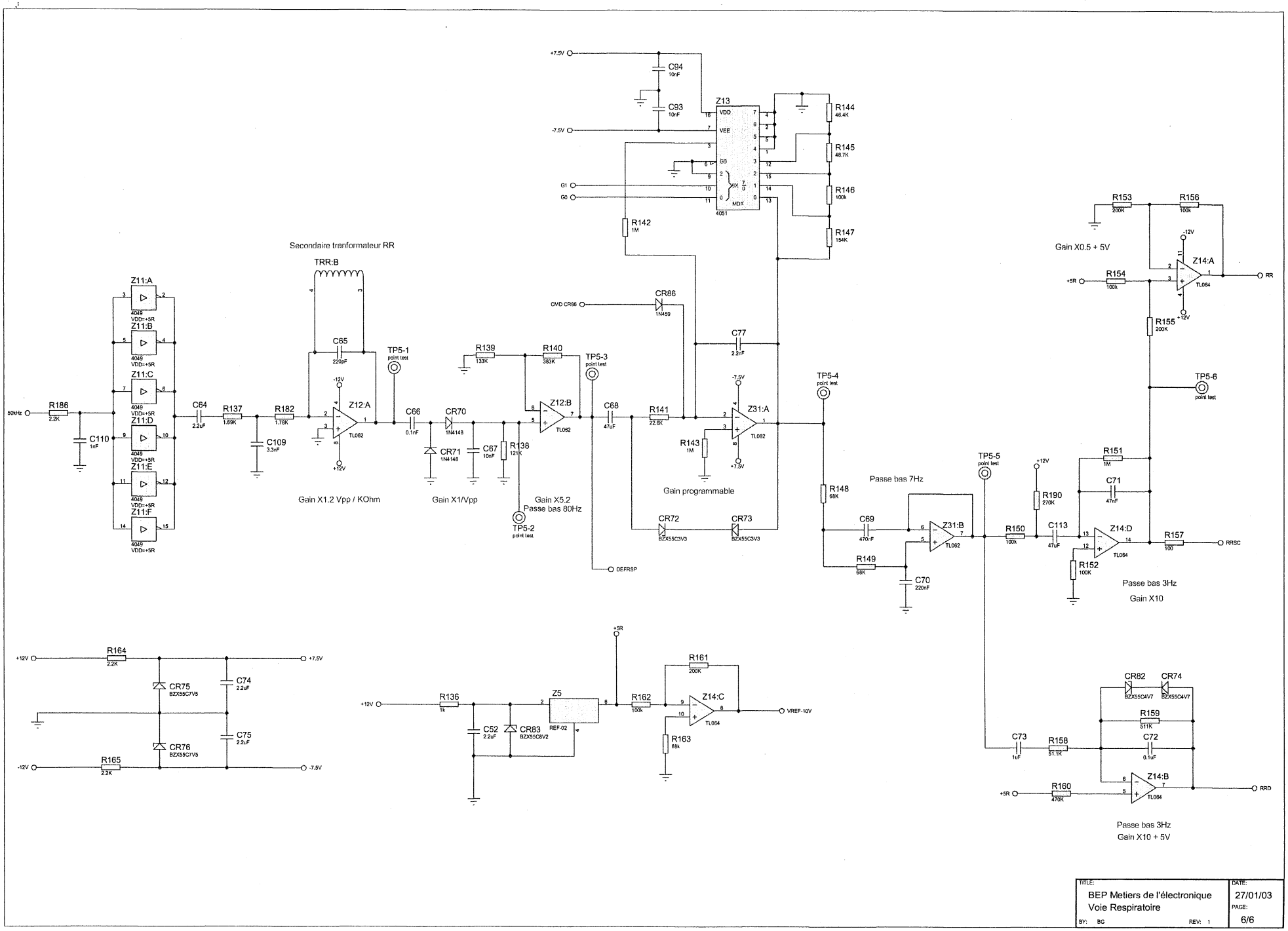
CORRIGÉ

Ces éléments de correction n'ont qu'une valeur indicative. Ils ne peuvent en aucun cas engager la responsabilité des autorités académiques, chaque jury est souverain.



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Dual 4-bit binary ripple counter | 74HC/HCT393

FEATURES

- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT393 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT393 are 4-bit binary ripple counters with separate clocks (1$\overline{CP}$ and 2 $\overline{CP}$) and master reset (1MR and 2MR) inputs to each counter. The operation of each half of the "393" is the same as the "93" except no external clock connections are required.
The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.
A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	n$\overline{CP}$ to nQ_0		12	20	ns
	nQ to nQ_{n+1}		5	6	ns
	nMR to nQ_n		11	15	ns
f_{max}	maximum clock frequency		99	53	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	23	25	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

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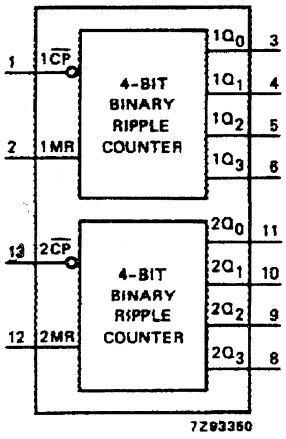

Fig.4 Functional diagram.

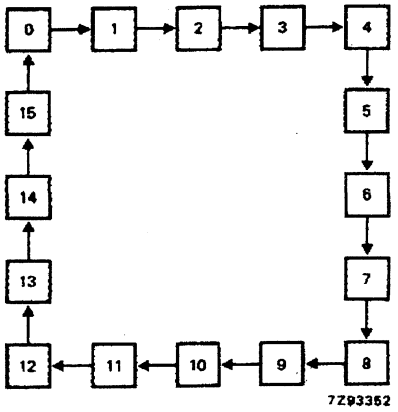

Fig.5 State diagram.

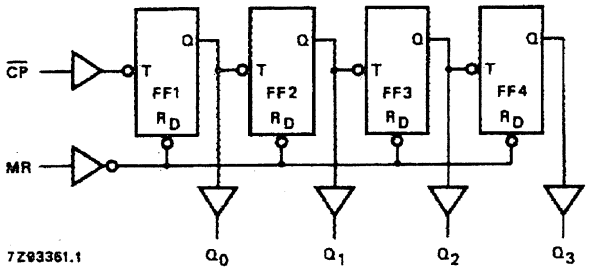

Fig.6 Logic diagram (one counter).

COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Notes

1. H = HIGH voltage level
   L = LOW voltage level

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DISPLAY COMMANDS

INSTRUCTION	CODE										DESCRIPTION
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1:Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.
2:Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter . Also returns display from being shifted to original position . DD RAM contents remain unchanged .
3:Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	I/D=1 : Increment I/D=0 : Decrement S=1 : Accompanies display shift
4:Display On/Off	0	0	0	0	0	0	1	D	C	B	I/D=1/0 : Display on/off I/D=0/1 : cursor on/off S=1 : Blink of cursor
5:Cursor /Display shift	0	0	0	0	0	1	S/C	R/L	*	*	S/C=1 : Display shift move S/C=0 : Cursor R/L=0 : Shift to left R/L=1 : Shift to right
6:Function Set	0	0	0	0	1	DL	N	F	*	*	DL=1 : 8 bits, DL=0 : 4 bits N=1 : 2 lines , N=0 : 1 line F=1 : 5*10 dots, F=0 : 5*8 dots
7: Set CG RAM Address	0	0	0	1	ACG						ACG : CG RAM address
8: Set DD RAM address	0	0	1	ADD							ADD : DD RAM address corresponds to cursor address
9:Read busy flag/address counter	0	1	BF	AC							BF=1 : Busy , BF=0 : Not busy AC : Address counter used for both of CG and DD RAM address
10:Write data	1	0	WRITE DATA								Write data to CG or DD RAM
11:Read data	1	1	READ DTAT								Read data from CG or DD RAM

★ Execution Time (Et) of Instruction : (Under condition of or fosc = 270 KHz)

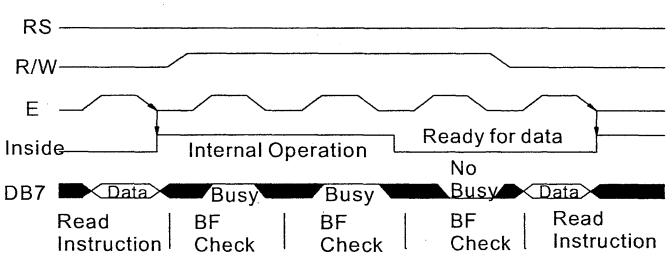
1 & 2 : Et=1.52ms

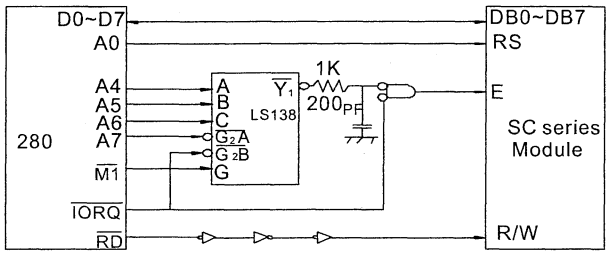
3 ~ 11 : Et=37μs

★ "* ": Either 0 or 1

CONNECTING BLOCK DIAGRAM

Example of interface with 8-bit MPU (Z80)





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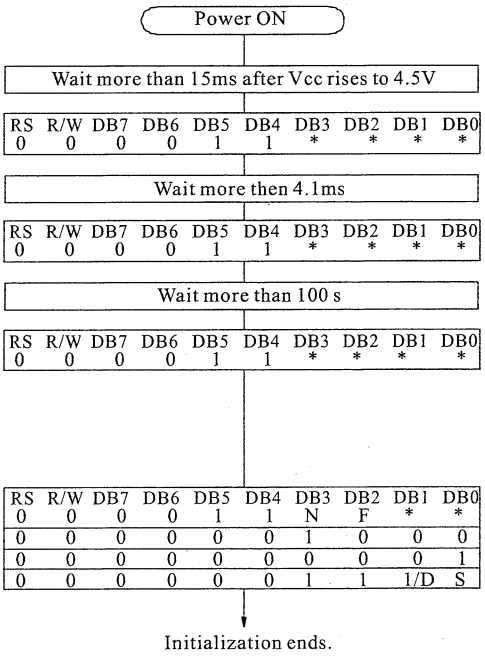
CONTENTS

INSTRUCTION BY INITIALIZING

If the power supply conditions for correctly operating the internal reset circuit are not met , initialization by instruction is required .

(1) When interface is 8 bits



When interface is 8-bit long.

Bf can not be checked before this instruction.
function set (interface is 8 bits long).

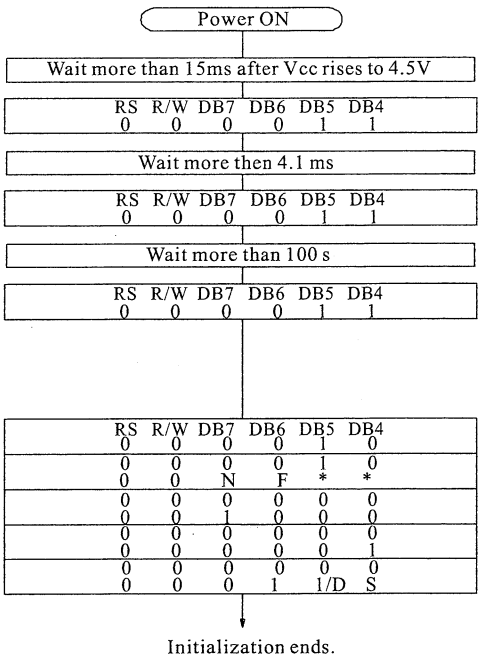
BF can be checked before this instruction.
function set (interface is 8 bits long).

BF can be checked before this instruction.
function set (interface is 8 bits long).

BF can not be checked after the following instructions.
When BF is not checked, the waiting time between instructions is longer than the execution time.

Function set (interface is 8 bits long. Specify the number of display lines and character font). The number of display lines and character can not be changed after wards.
Display OFF
Display Clear
Entry Mode Set

(1) When interface is 4 bits



When interface is 4-bit long.

BF can not be checked before this instruction.
function set (interface is 4 bits long).

BF can not be checked before this instruction.
function set (interface is 4 bits long).

BF can be checked before this instruction.
function set (interface is 4 bits long).

BF can be checked after the following instructions.
When BF is not checked, the waiting time between instructions is longer than the execution time.

Function set (interface is 4 bits long. Specify the number of display lines and character font). The number of display lines and character can not be changed after wards.
Display OFF

Display Clear

Entry Mode Set

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