CORRIGÉ

Ces éléments de correction n'ont qu'une valeur indicative. Ils ne peuvent en aucun cas engager la responsabilité des autorités académiques, chaque jury est souverain.

8-channel analog multiplexer/demultiplexer 74HC/HCT4051

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	Z	common input/output
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S_0 to S_2	select inputs
13, 14, 15, 12, 1, 5, 2, 4	Y_0 to Y_7	independent inputs/outputs
16	V_{CC}	positive supply voltage

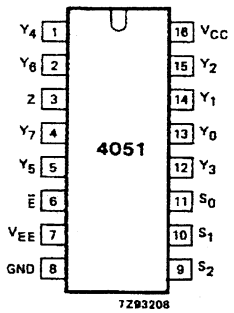

Fig.1 Pin configuration.

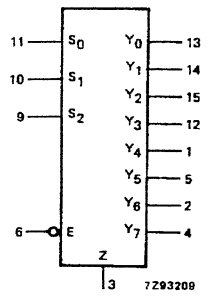

Fig.2 Logic symbol.

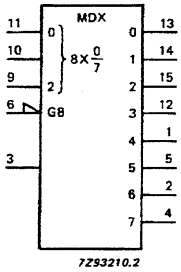

Fig.3 IEC logic symbol.

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8-channel analog multiplexer/demultiplexer 74HC/HCT4051

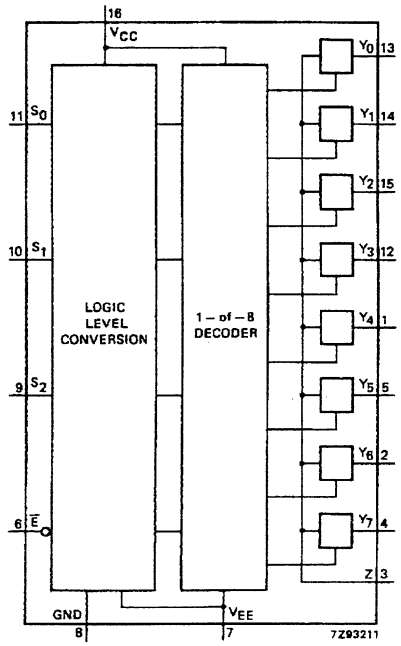

Fig.4 Functional diagram.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

FUNCTION TABLE

INPUTS				channel ON
$\overline{E}$	S_2	S_1	S_0	
L	L	L	L	$Y_0 - Z$
L	L	L	H	$Y_1 - Z$
L	L	H	L	$Y_2 - Z$
L	L	H	H	$Y_3 - Z$
L	H	L	L	$Y_4 - Z$
L	H	L	H	$Y_5 - Z$
L	H	H	L	$Y_6 - Z$
L	H	H	H	$Y_7 - Z$
H	X	X	X	none

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

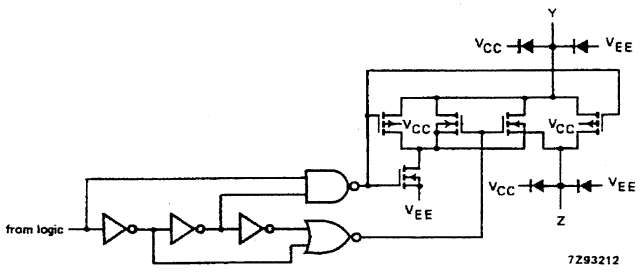

Fig.5 Schematic diagram (one switch).

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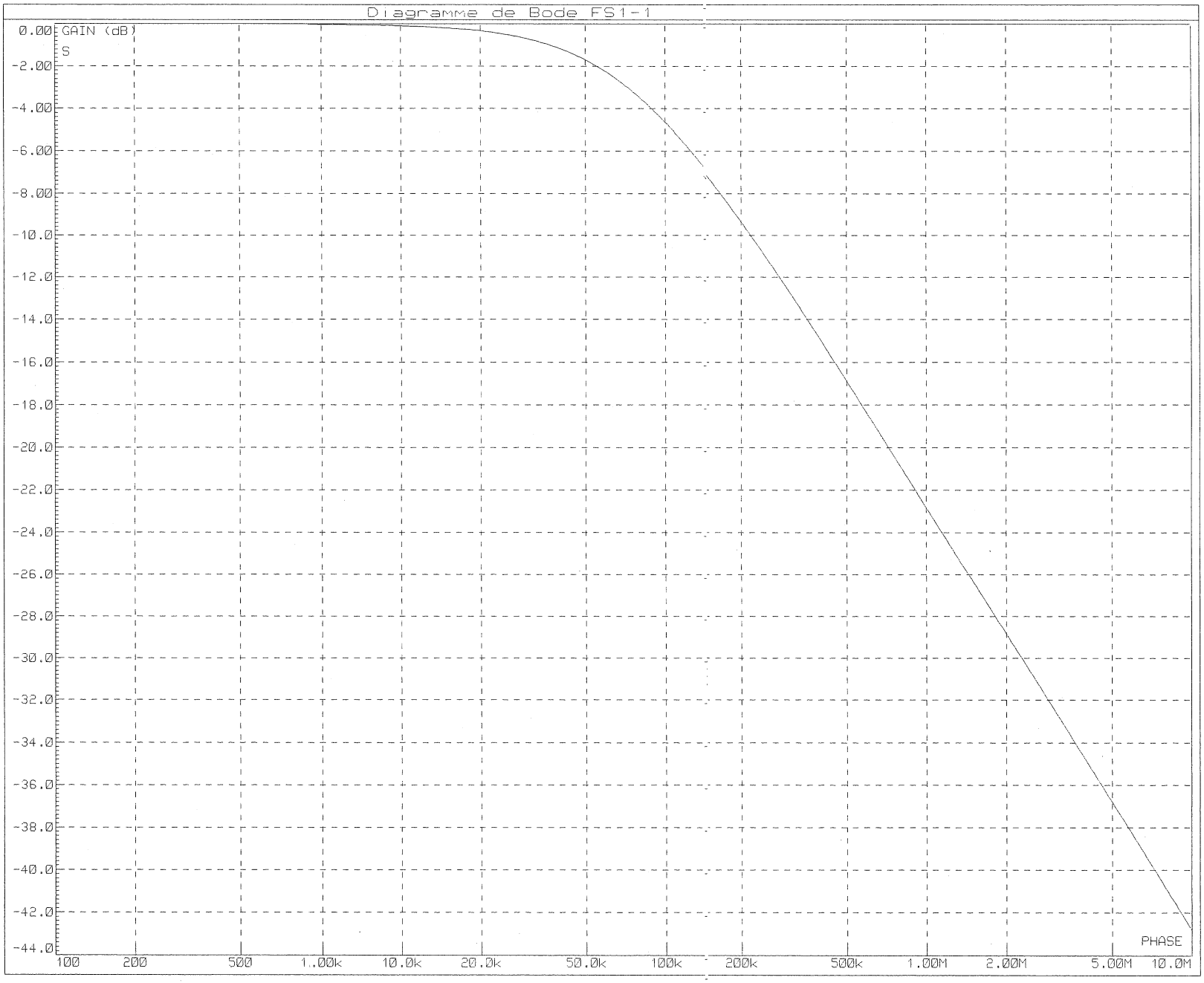
Diagramme de Bode FS1-1
GAIN (dB)
S
0.00
-2.00
-4.00
-6.00
-8.00
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
-24.0
-26.0
-28.0
-30.0
-32.0
-34.0
-36.0
-38.0
-40.0
-42.0
-44.0
100
200
500
1.00k
10.0k
20.0k
50.0k
100k
200k
500k
1.00M
2.00M
5.00M
10.0M
PHASE

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SN54LS138, SN54S138, SN74LS138, SN74S138A
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SDLS014

DECEMBER 1972—REVISED MARCH 1988

- **Designed Specifically for High-Speed:**
  Memory Decoders
  Data Transmission Systems
- **3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Schottky-Clamped for High Performance**

description

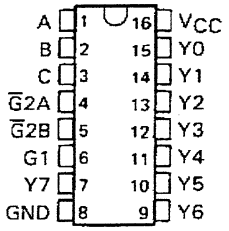
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these docoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138, SN54S138, and SN74S138A decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

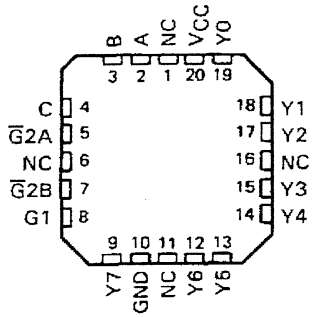
All of these decoder/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design.

The SN54LS138 and SN54S138 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS138 and SN74S138A are characterized for operation from 0°C to 70°C.

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138A . . . D OR N PACKAGE
(TOP VIEW)

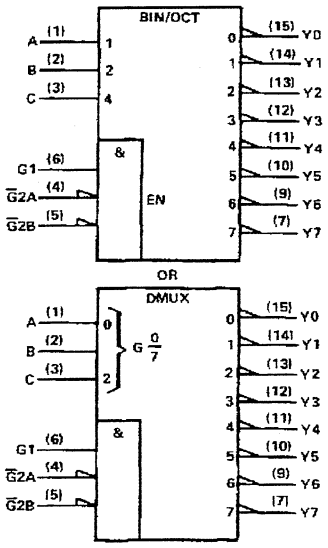


SN54LS138, SN54S138 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

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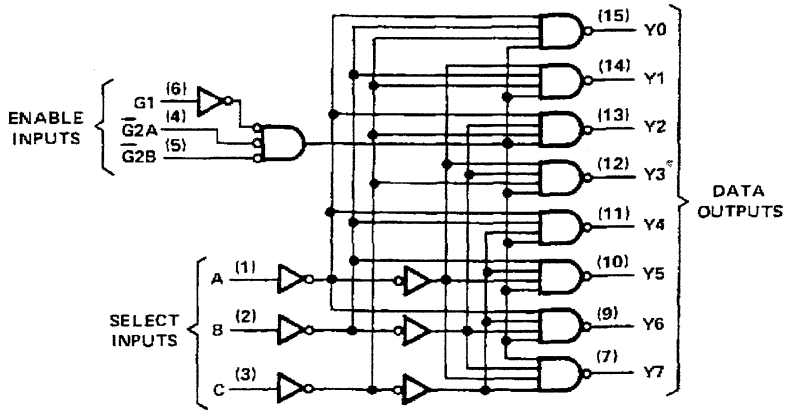
logic diagram and function table

'LS138, SN54S138, SN74S138A



Pin numbers shown are for D, J, N, and W packages.

'LS138, SN54138, SN74S138A
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$
H = high level, L = low level, X = irrelevant

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CMOS 8-Bit 8-Channel Data Acquisition System

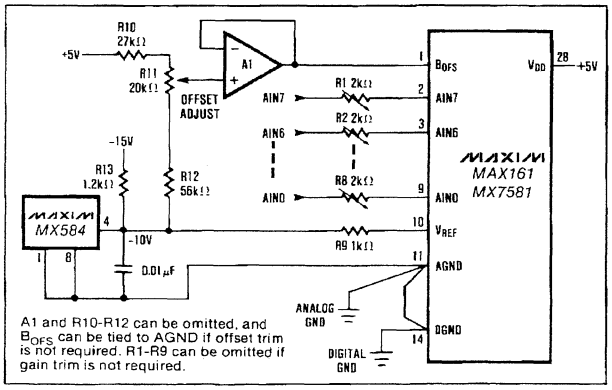

Figure 5. Unipolar (0 to +10V) Operation

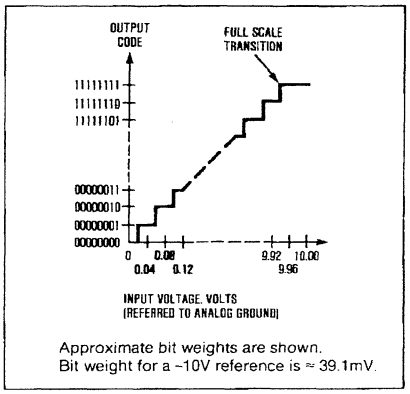

Figure 6. Unipolar (0 to +10V) Transfer Characteristic

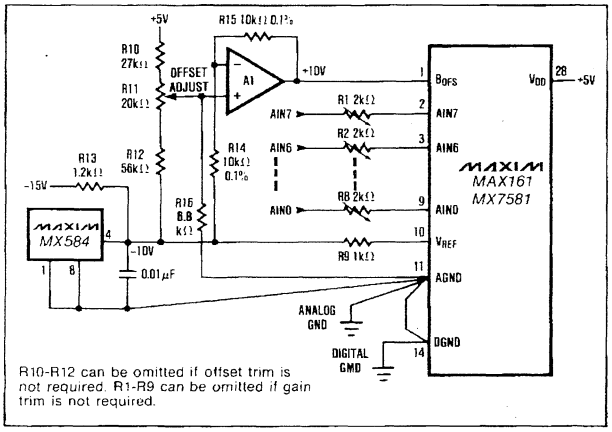

Figure 7. Unipolar (0 to -10V) Operation

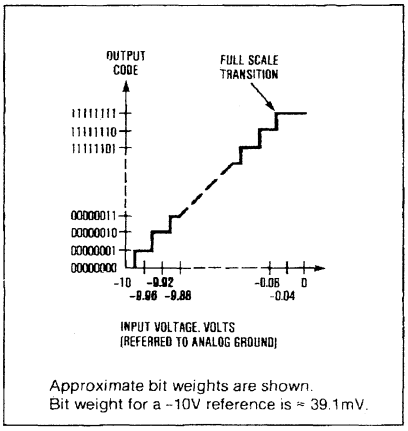

Figure 8. Unipolar (0 to -10V) Transfer Characteristic

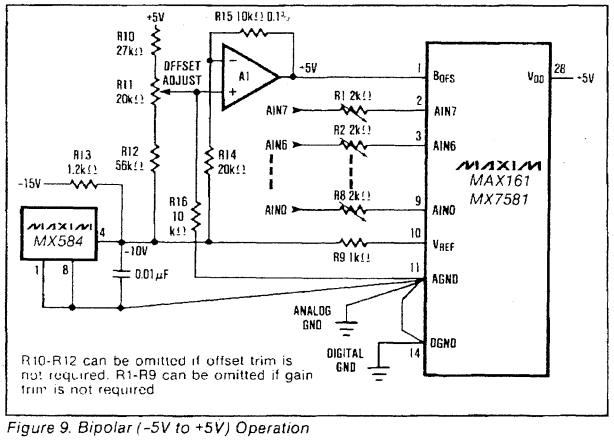

Figure 9. Bipolar (-5V to +5V) Operation

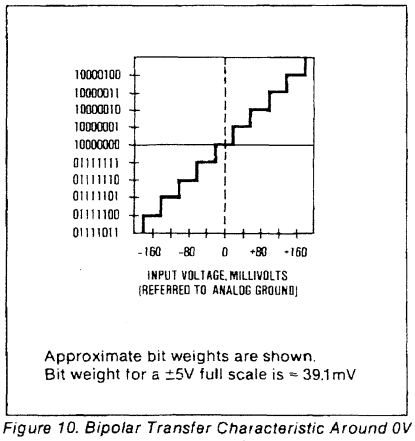

Figure 10. Bipolar Transfer Characteristic Around 0V

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CMOS 8-Bit 8-Channel Data Acquisition System

Detailed Description

Basic Operation

The MAX161 and MX7581 sequentially convert analog signals on 8 input channels into separate 8-bit data words. The data is continually updated in on-chip RAM, with each channel's conversion result assigned to a separate RAM address. Consequently, the conversion process is user transparent in that output data is read directly from RAM. The device can run directly from a microprocessor clock (6800 type systems) or control signal (ALE in 8085 type systems). A functional diagram of the MAX161 and MX7581 is shown on the front page.

A/D Conversion

Internally, the conversion process is divided into 10 phases, each 8 clock periods long. In the first phase, the input multiplexer is decremented and the control logic is reset. $\overline{STAT}$ (pin 12) goes low for 8 clock cycles at the beginning of this period. ($\overline{STAT}$ also goes low for 72 clock periods after channel 1 is converted). The successive approximation A/D conversion then takes place during phases 2 through 9. Finally, data is loaded into RAM during phase 10.

A single channel conversion takes 80 input clock periods while a complete scan through all channels requires 640 clock periods. Internal start-up logic initializes the converter within 800 clock periods after power is applied.

Digital Interface

Channel Selection

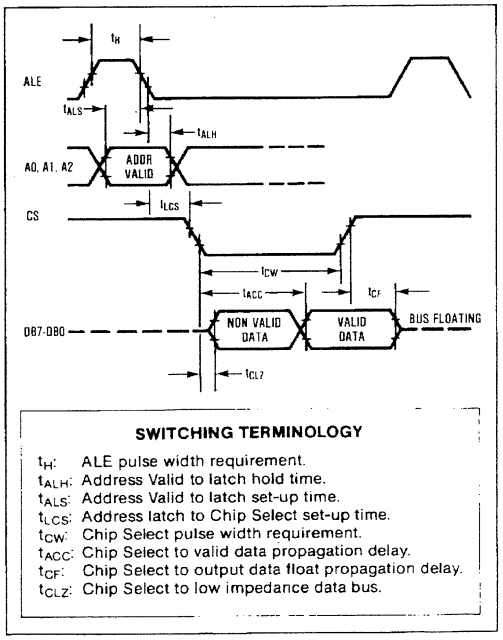
Table 1 shows the truth table for channel selection. RAM locations are addressed by AO-A2. In systems with a multiplexed address/data bus, the address is latched by ALE (pin 16). Alternatively, when address and data busses are separate, the address latches can be made transparent by tying ALE HIGH.

Table 1:
Channel Selection Truth Table

A2	A1	A0	ALE	CHANNEL DATA TO BE READ
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Timing And Control

Control timing for the MAX161 and MX7581 is shown in Figure 1. When CS (pin 13) is HIGH, the three-state data drivers are in their high impedance state. The drivers switch to the active state when $\overline{CS}$ goes LOW. Output data is valid after time t_{ACC}.



SWITCHING TERMINOLOGY

t_H: ALE pulse width requirement.
t_{ALH}: Address Valid to latch hold time.
t_{ALS}: Address Valid to latch set-up time.
t_{LCS}: Address latch to Chip Select set-up time.
t_{CW}: Chip Select pulse width requirement.
t_{ACC}: Chip Select to valid data propagation delay.
t_{CF}: Chip Select to output data float propagation delay.
t_{CLZ}: Chip Select to low impedance data bus.

Figure 1. Interface Timing Diagram

Data Read Operation

The MAX161 and MX7581 continuously scan and convert analog input signals without regard to the channel being selected for data output. The on-chip RAM and contention logic allow data to be read asynchronously with respect to the conversion process. The output data (RAM contents) is simply the most recent conversion result for the selected channel.

Automatic Interleaved DMA is provided by internal logic to ensure that memory updates do not take place when the memory is being addressed by a microprocessor. RAM is normally updated on a rising clock edge, 6 clock periods prior to $\overline{STAT}$ going LOW, provided $\overline{CS}$ is HIGH (i.e. data is not being read). If $\overline{CS}$ is LOW (read operation in progress), then the memory update is delayed by 3 clock periods. By delaying the update, data will not be written in RAM during a READ as long as $\overline{CS}$ is kept shorter than 3 clock periods. The possibility of a "contention" error with an asynchronous READ is therefore eliminated if $\overline{CS}$ is less than 3 clock periods long. Although asynchronous reading errors are eliminiated with this feature, it in no way restricts compatibility with other manufacturers' MX7581s.

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