B.T.S. ELECTRONIQUE

Session 2005

ETUDE D'UN SYSTEME TECHNIQUE

SYSTEME DE SERRAGE AUTOMATISE MOD 5200

Dossier documentation constructeur

SOMMAIIRE

19-0218; Rev 3; 6/01

MAXIM

Microprocessor Supervisory Circuits

MAX690/91/92/93/94/95

General Description

The MAX690 Family of supervisory circuits reduce the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include µP reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX690 Family significantly improves system reliability and accuracy compared to that obtainable with separate ICs or discrete components.

The MAX690, MAX692 and MAX694 are supplied in 8-pin packages and provide four functions:
1) A Reset output during power-up, power-down and brownout conditions.
2) Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
3) A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
4) A 1.3V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

The MAX691, MAX693 and MAX695 are supplied in 16-pin packages and perform all MAX690/692/694 functions, plus:
1) Write protection of CMOS RAM or EEPROM.
2) Adjustable reset and watchdog timeout periods.
3) Separate outputs for indicating a watchdog timeout, backup-battery switchover, and low V_{CC}.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Features

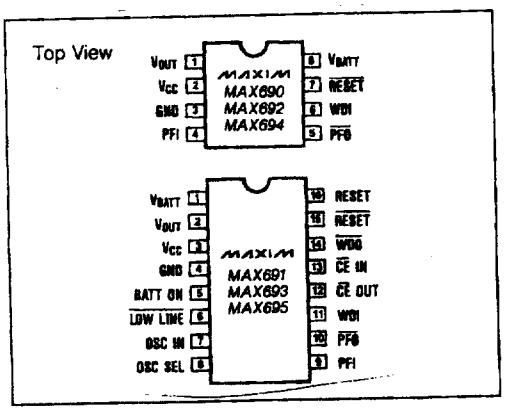
- **Precision Voltage Monitor**
  4.65V in MAX690, MAX691, MAX694 and MAX695
  4.40V in MAX692 and MAX693
- **Power OK/Reset Time Delay – 50, 200ms, or adjustable**
- **Watchdog Timer – 100ms, 1.6 sec, or adjustable**
- **Minimum Component Count**
- **1µA Standby Current**
- **Battery Backup Power Switching**
- **Onboard Gating of Chip Enable Signals**
- **Voltage Monitor for Power Fail or Low Battery Warning**

Ordering Information

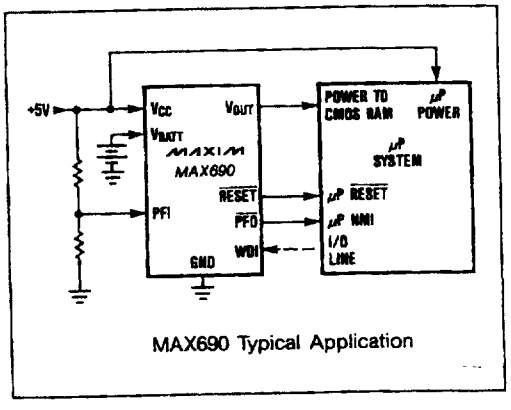
PART	TEMP. RANGE	PIN-PACKAGE
MAX690CPA	0°C to +70°C	8 Lead Plastic DIP
MAX690C/D	0°C to +70°C	Dice*
MAX690EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX690EJA	-40°C to +85°C	8 Lead CERDIP
MAX690MJA	-55°C to +125°C	8 Lead CERDIP
MAX691CPE	0°C to +70°C	16 Lead Plastic DIP
MAX691CWE	0°C to +70°C	16 Lead Wide SO
MAX691C/D	0°C to +70°C	Dice*
MAX691EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX691EWE	-40°C to +85°C	16 Lead Wide SO
MAX691EJE	-40°C to +85°C	16 Lead CERDIP
MAX691MJE	-55°C to +125°C	16 Lead CERDIP

Ordering Information continued on last page.
**Contact factory for dice specifications.*

Pin Configuration



Typical Operating Circuit



MAX690 Typical Application

Microprocessor Supervisory Circuits

Pin Description

NAME	PIN		FUNCTION
	MAX690/ 692/694	MAX691/ 693/695	
V_{CC}	2	3	The +5V input.
V_{BATT}	8	1	Backup battery input. Connect to Ground if a backup battery is not used.
V_{OUT}	1	2	The higher of V_{CC} or V_{BATT} is internally switched to V_{OUT}. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used. Connect a 0.1µF or larger bypass capacitor to V_{OUT}.
GND	3	4	0V Ground reference for all signals.
$\overline{RESET}$	7	15	$\overline{RESET}$ goes low whenever V_{CC} falls below either the reset voltage threshold or the V_{BATT} input voltage. The reset threshold is typically 4.65V for the MAX690/ 691/694/695, and 4.4V for the MAX692 and MAX693. $\overline{RESET}$ remains low for 50ms after V_{CC} returns to 5V. (except 200ms in MAX694/695). $\overline{RESET}$ also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table 1.
WDI	6	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	4	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{OUT} when not used. See Figure 1.
$\overline{PFO}$	5	10	$\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and $\overline{PFO}$ goes low when V_{CC} is below V_{BATT}.
$\overline{CE}$ IN	—	13	The input to the $\overline{CE}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{CE}$ OUT	—	12	$\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold (4.65V for MAX691 and MAX695, 4.4V for MAX693). See Figure 6.
BATT ON	—	5	BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 25mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}.
$\overline{LOW\ LINE}$	—	6	$\overline{LOW\ LINE}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. See Figure 6, Reset Timing.
RESET	—	16	RESET is an active high output. It is the inverse of $\overline{RESET}$.
OSC SEL	—	8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3µA internal pullup. See Table 1.
OSC IN	—	7	When OSC SEL is low, OSC IN can be driven by an external clock to adjust both the reset delay and the watchdog timeout period. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 8. When OSC SEL is high or floating, OSC IN selects between fast and slow Watchdog timeout periods.
$\overline{WDO}$	—	14	The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the Watchdog timeout period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low.

FAIRCHILD SEMICONDUCTOR™

September 1983
Revised February 1999

MM74HC393
Dual 4-Bit Binary Counter

General Description

The MM74HC393 counter circuits contain independent ripple carry counters and utilize advanced silicon-gate CMOS technology. The MM74HC393 contains two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the HIGH-to-LOW transition (negative edge) of the clock input, and each has an independent clear input. When clear is set HIGH all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads. This counter is functionally as well as pin equivalent to the 74LS393. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 13 ns (Ck to Q_A)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 µA
- Low quiescent supply current: 80 µA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

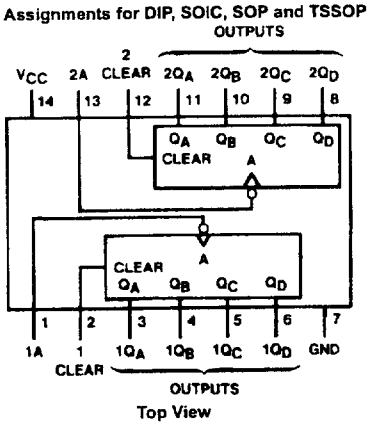
Ordering Code:

Order Number	Package Number	Package Description
MM74HC393M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC393SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC393MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC393N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

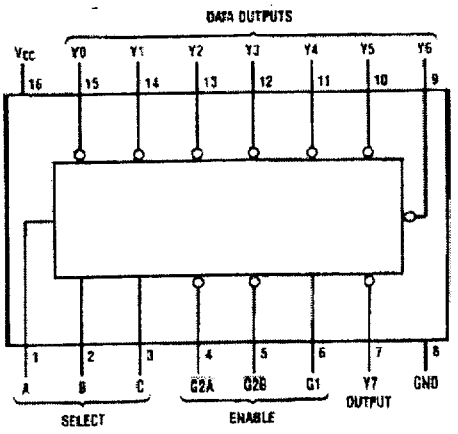
Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



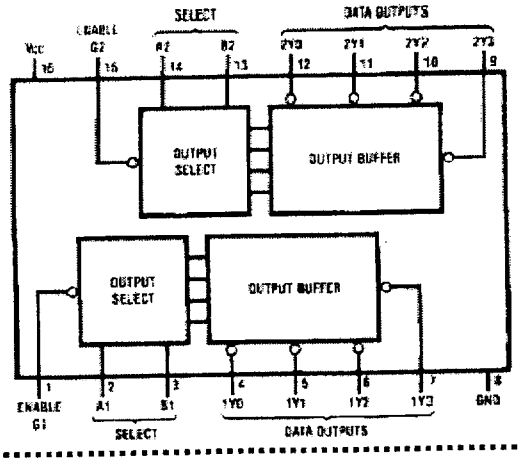
Top View

74HC138



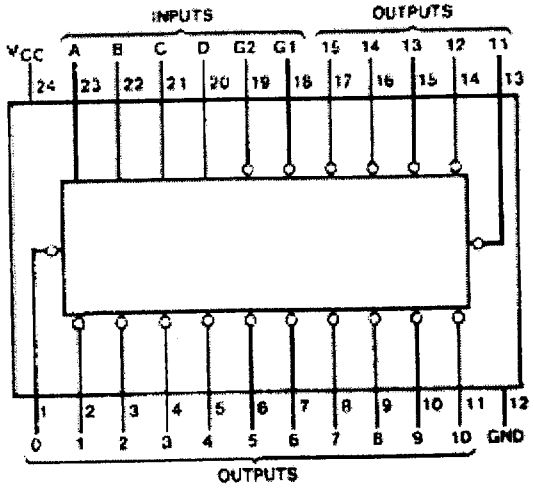
Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$ (Note 1)	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

74HC139



Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

74HC154



Inputs						Low
$\overline{G1}$	$\overline{G2}$	D	C	B	A	Output (Note 1)
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	10
L	L	H	L	H	H	11
L	L	H	H	L	L	12
L	L	H	H	L	H	13
L	L	H	H	H	L	14
L	L	H	H	H	H	15
L	H	X	X	X	X	—
H	L	X	X	X	X	—
H	H	X	X	X	X	—

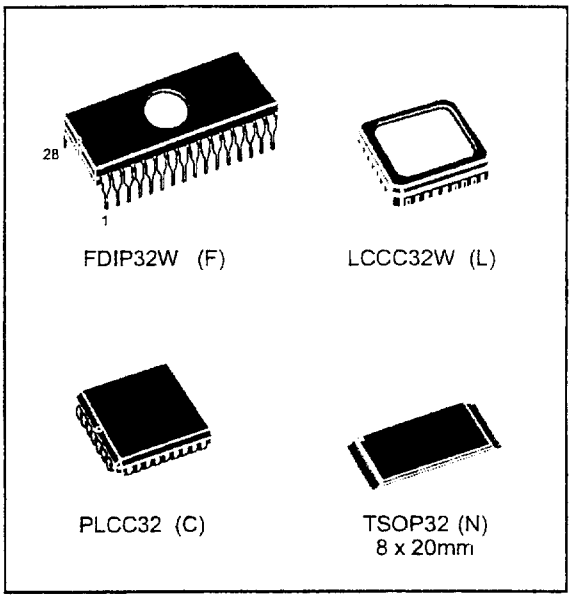
Note 1: All others HIGH

SGS-THOMSON MICROELECTRONICS

M27C2001

2 Megabit (256K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C2001 is a high speed 2 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C2001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

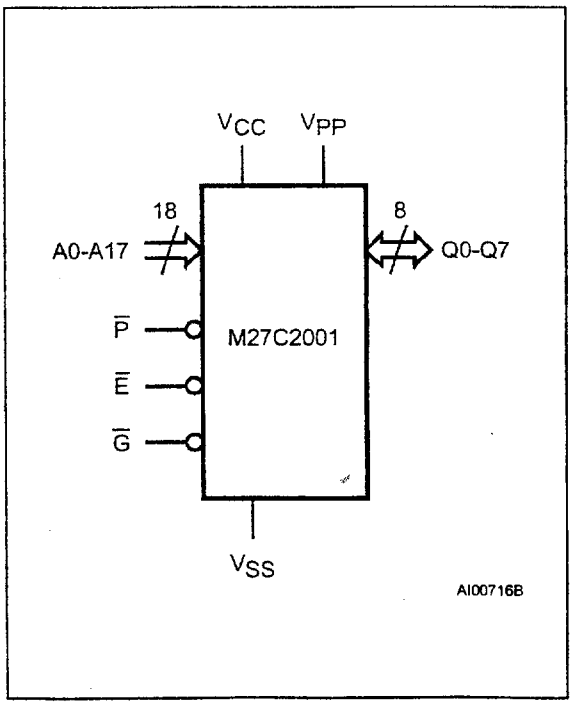


Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

SONY CXK581000ATM/AYM/AM/AP-70LLX/10LLX

131,072-word × 8-bit High-Speed CMOS Static RAM

Description

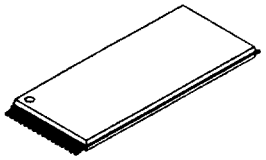
The CXK581000ATM/AYM/AM/AP are high speed CMOS static RAMs organized as 131,072-words-by-8-bits.

A polysilicon TFT cell technology realizes extremely low stand-by current and higher data retention stability.

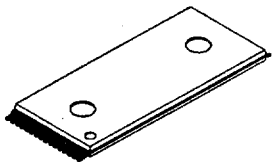
Special features are low power consumption, high speed and a broad package line-up.

The CXK581000ATM/AYM/AM/AP are suitable RAMs for portable equipment with battery backup.

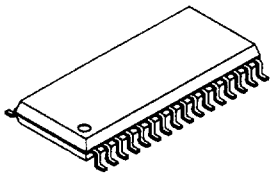
CXK581000ATM
32-pin TSOP (Plastic)



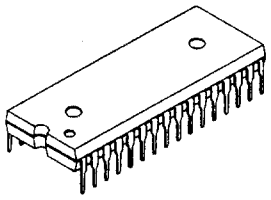
CXK581000AYM
32-pin TSOP (Plastic)



CXK581000AM
32-pin SOP (Plastic)



CXK581000AP
32-pin DIP (Plastic)



Features

- Extended operating temperature range: (–25°C to +85°C)
- Fast access time: –70LLX 70ns (max.)
  –10LLX 100ns (max.)
- Low standby current: 40µA (max.)
- Low data retention current: 24µA (max.)
- Single +5V supply: +5V ± 10%
- Low voltage data retention: 2.0V (min.)
- Broad package line-up

ATM/AYM	8mm × 20mm 32 pin TSOP pkg.
AM	525mil 32 pin SOP package
AP	600mil 32 pin DIP package

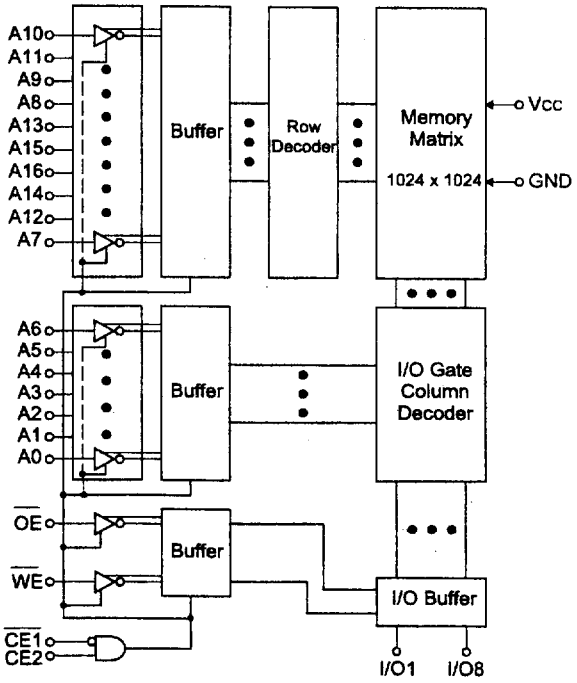
Functions

131072 word × 8 bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram



E94429–TE

• Read Cycle ($\overline{WE}$ = "H")

Item	Symbol	-70LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	100	—	ns
Address access time	t_{AA}	—	70	—	100	
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	70	—	100	
Chip enable access time (CE2)	t_{CO2}	—	70	—	100	
Output enable to output valid	t_{OE}	—	40	—	50	
Output hold from address change	t_{OH}	10	—	10	—	
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1},t_{LZ2}	10	—	10	—	
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*,t_{HZ2}*	—	25	—	35	
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	25	—	35	

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write Cycle

Item	Symbol	-70LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	100	—	ns
Address valid to end of write	t_{AW}	60	—	70	—	
Chip enable to end of write	t_{CW}	60	—	70	—	
Data to write time overlap	t_{DW}	30	—	40	—	
Data hold from write time	t_{DH}	0	—	0	—	
Write pulse width	t_{WP}	50	—	70	—	
Address setup time	t_{AS}	0	—	0	—	
Write recovery time ($\overline{WE}$)	t_{WR}	5	—	5	—	
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	
Output active from end of write	t_{OW}	10	—	10	—	
Write to output in high Z	t_{WHZ}*	—	25	—	30	

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

FAIRCHILD SEMICONDUCTOR®

September 1983
Revised July 2002

MM74HC164
8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM74HC164 utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A LOW at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

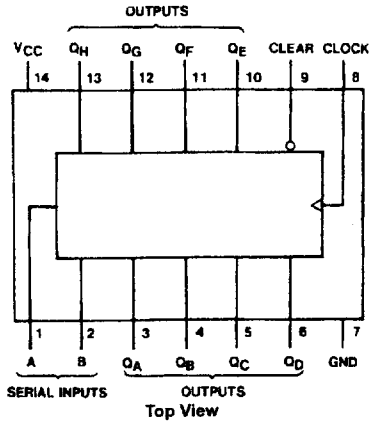
- Typical operating frequency: 50 MHz
- Typical propagation delay: 19 ns (clock to Q)
- Wide operating supply voltage range: 2V to 6V
- Low input current: 1 µA maximum
- Low quiescent supply current: 80 µA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Ordering Code:

Order Number	Package Number	Package Description
MM74HC164M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC164MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC164N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Top View

Truth Table

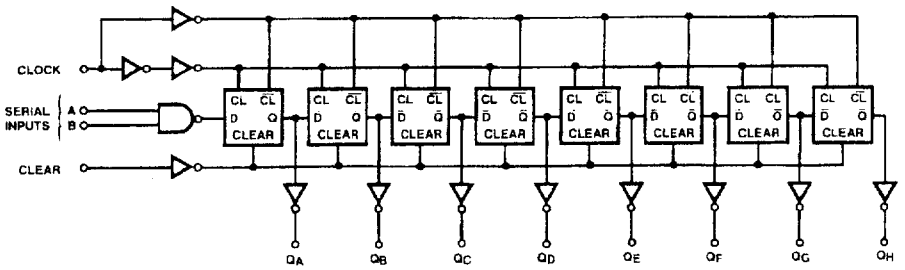
Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = HIGH Level (steady state), L = LOW Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW-to-HIGH level.
Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

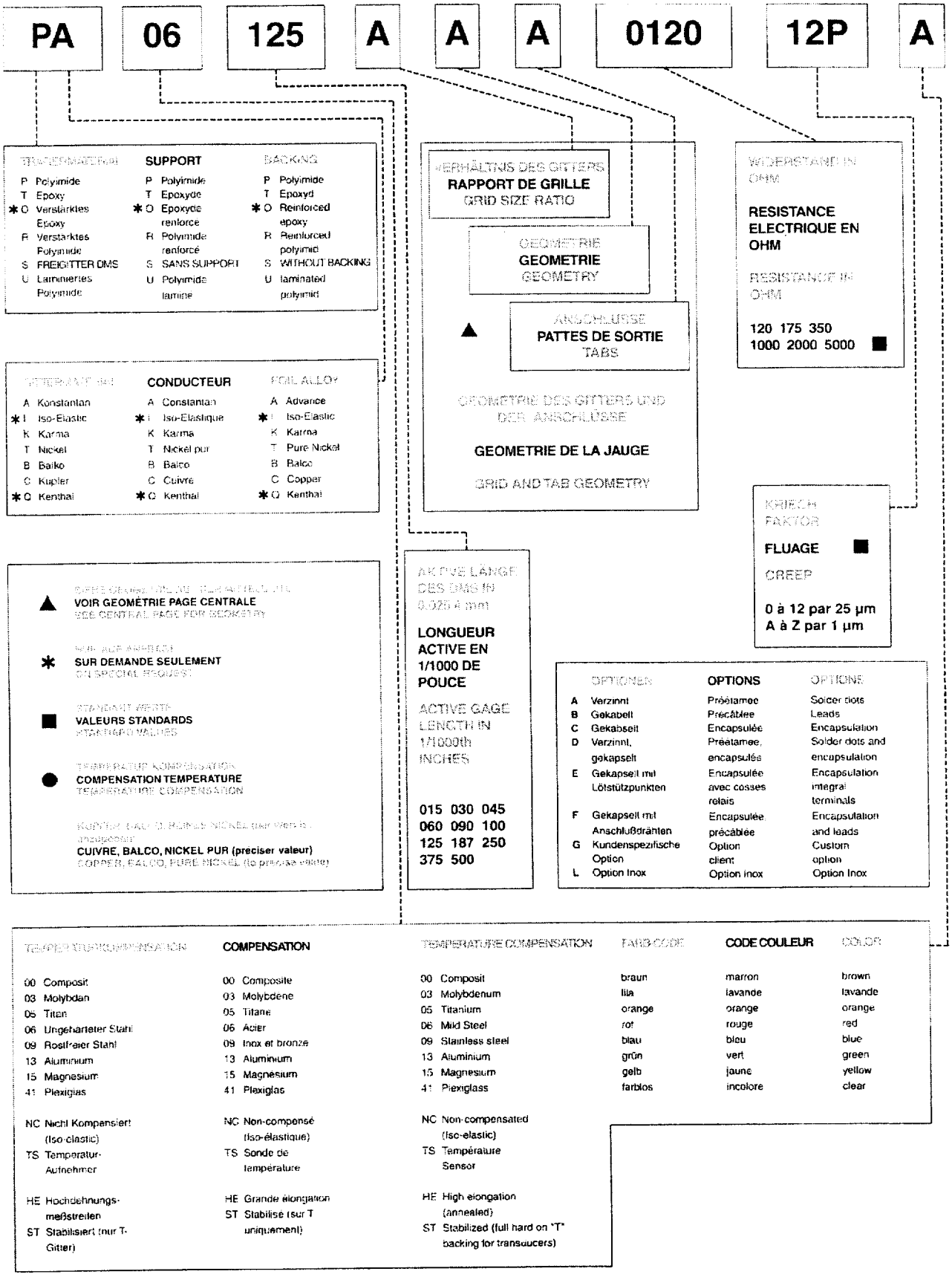
 DS005315 www.fairchildsemi.com

MM74HC164

Logic Diagram

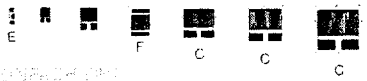


BESTELLCODE **CODIFICATION** CODING SYSTEM



RAPPORT DE GRILLE

2 code G



JAUGE SIMPLE
SINGLE GAGE

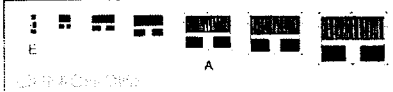
TAILLE / SIZE	015	030	045	060	090	100	125
GEOMETRIE	A						
SORTIES	G C E F						
TYP DESIGNATION REFERENCE	TA XX 125 GAC 350 - 7						

JAUGES DOUBLES
DOUBLE GAGES

TAILLE / SIZE	015	030	045	060
GEOMETRIE	B			
SORTIES	E A			
TYP DESIGNATION REFERENCE	TA XX 125 GBA 350 - 7			

RAPPORT DE GRILLE

3 code H



JAUGE SIMPLE
SINGLE GAGE

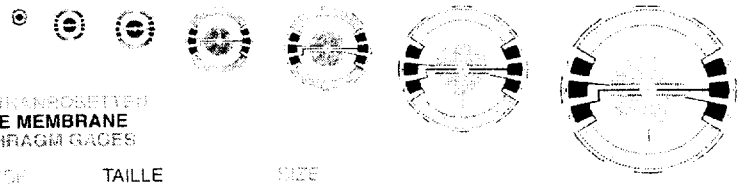
TAILLE / SIZE	015	030	045	060	090	100	125
GEOMETRIE	A						
SORTIES	E A						
TYP DESIGNATION REFERENCE	TA XX 125 HAA 350 - 7						

RAPPORT DE GRILLE

4 code I

JAUGE SIMPLE
SINGLE GAGE

TAILLE / SIZE	015	030	045	060	090	100	125
GEOMETRIE	A						
SORTIES	A						
TYP DESIGNATION REFERENCE	TA XX 125 IAA 350 - 7						



JAUGE MEMBRANE
DIAPHRAGM GAGES

TAILLE / SIZE	090	182	228	364	455	683	910
GEOMETRIE	D						
SORTIES	U						
TYP DESIGNATION REFERENCE	TA XX 455 ODU 350 - 7						

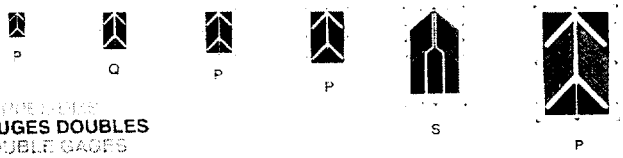
RAPPORT DE GRILLE

0 code O

JAUGE SIMPLE 45°
SIMPLE GAGE 45

TAILLE / SIZE	250	125	100	090	060
GEOMETRIE	F				
SORTIES	O				
TYP DESIGNATION REFERENCE	TA XX 125 FFO 350 - 7				

TAILLE / SIZE	250	125	100	090	060
GEOMETRIE	G				
SORTIES	O				
TYP DESIGNATION REFERENCE	TA XX 125 FGO 350 - 7				



JAUGES DOUBLES
DOUBLE GAGES

TAILLE / SIZE	060	090	100	125	187	250
GEOMETRIE	H					
SORTIES	P Q S					
TYP DESIGNATION REFERENCE	TA XX 125 FHP 350 - 7					

Dieses Programm zeigt die verschiedenen DMS, die wir herstellen. Lieferbar in Konstantan, Karma, Iso-elastischer Folie, Kenthal, Kupfer, Balco und Nickel auf Polyimide-oder Epoxy-Träger mit Selbst-Temperaturkompensation von 0-41.

Ce programme présente les différentes jauges que nous fabriquons. Elles peuvent être fabriquées en constantan, en karma, en isoelastic ou en kenthal, en cuivre, balco ou nickel sur support polyimide ou époxy avec toutes auto-compensations de 0 à 41.

This Program shows our strain gage range, all gages can be delivered in Advance, Karma, Iso-elastic foil, Kenthal, Copper, Balco and Nickel with polyimide or epoxy backing, and self-temperature compensation from 0 to 41.

TOUS LES DESSINS SONT À L'ECHELLE 1
SCALE DRAWINGS