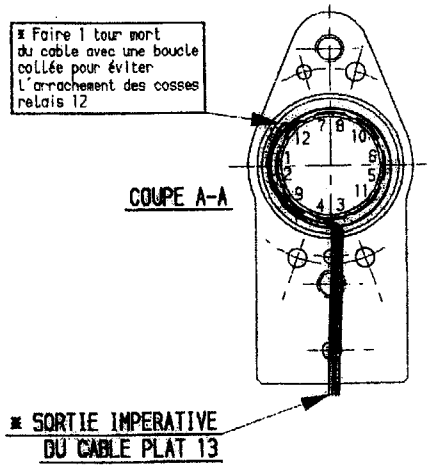
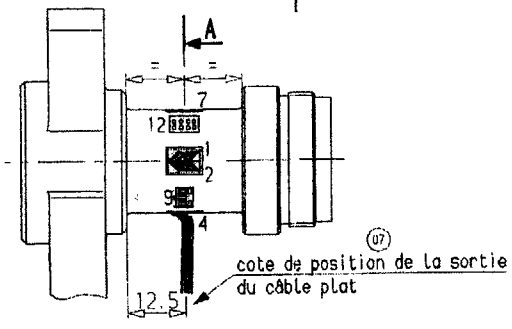
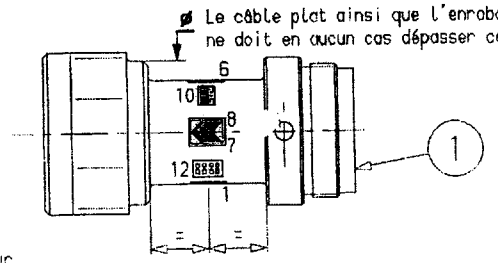






OPERATIONS DEMANDEES :

- Collage des jauges
- Cablage
- Les jauges sont collées avec de la colle M610
- Encapsulage des jauges par 2 couches de colle M610
- Enrobage GK 20 du capteur complet
- Câblage des fils de sortie (soudure carte + connecteur)

NOTA : offset ≤ 15µV/V

DESIGNATIONS : (07)

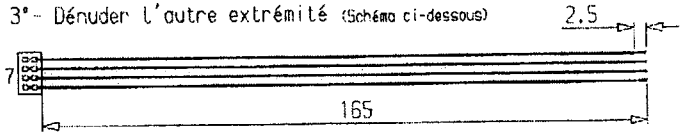
- 1 à 8 : 920.789 -> 4 jauges TA-13-125-FHP 350
- 9 à 10 : 920.793 -> 2 jauges PTTS 060 CC 50
- 11 : 920.791 -> Jauge TA-13-125-FHP 350
- 12 : 916.049 -> 4 cosses relais FCNC 050 SP4
- 13 : 916.564 -> câble plat Lg 165mm (4X EPDX 4X0)
- 14 : carte convertisseur 918.727

CABLAGE DES FILS DE SORTIE :

1°- Couper le câble plat 13 à 165 mm de longueur.

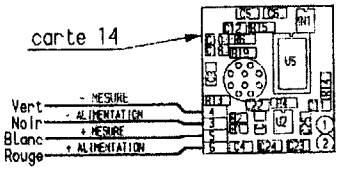
2°- Le souder aux cosses relais 12

3°- Dénuder l'autre extrémité (Schéma ci-dessous)



4°- Faire 1 tour mort avec une boucle collée et respecter la sortie des fils impérativement. (Voir schémc ci-dessus *)

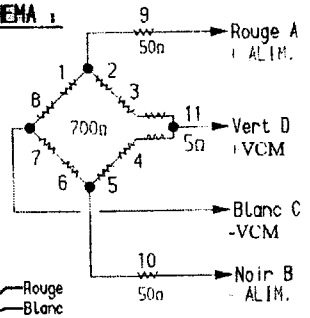
5°- Souder le câble plat 13 à l'ensemble carte 14 :
(Schéma ci-dessous)



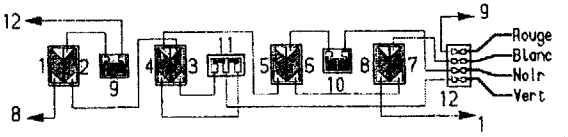
ATTENTION : Dans tous les cas la Longueur libre des fils (entre l'enrobage et la carte convertisseur) devra être au minimum de 75mm

PLAN NON APPROUVE INDICE ANNULE ET REMPLACE TOUS PLANS EN CIRCULATION REMPLACE PAR CETTE EDITION 08 JAN. 2001

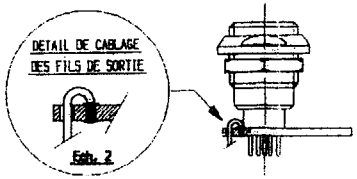
SCHEMA :



CABLAGE CAPTEUR DEPLIE :



IMPORTANT : Avant tout changement : composants, câblage... s'en référer impérativement au RDM !



Ind. Note	Partition	Modification	Date	Visa
05	.	Chgt d'indice par analogie au n°615 570393 2 ind. 05	001220	ALG
08	.	Chgt d'indice par analogie au n°615 570393 2 ind. 03	000908	ALG
07	.	Passage de 2 jauges doubles à 4 jauges doubles	991018	ALG
06	.	Chgt d'indice par analogie au n°615 570393 2	990505	ALG
05	.	Ajouter nota concernant la longueur des fils	981215	BH
04	.	Positionnement de la sortie du câble plat	980530	DD

Rep No	Piece No/Part No	Plan No/Drawing No	Qty/Qty	Designation
1	.	615 570393 2	1	Bride élément déformant

GEORGES RENAULT

Description: ELEMENT DEFORMANT EQUIPE 1.6mV/V pour 25Nm EM35-20J
Matière/Material: AU4G1 T351 (2024 T351 uniquement)
Traitement/Treatment:
Comp. code: GRE
Format: A3

Tolerances par défaut / Tolerances by default: ISO 2768-f
Usinage général / Gen. machining: 1.6
Echelle / Scale: 1/1
Dessiné par / Drawn by: ALG
Poids / Weight:
Vérif. Std. / Std. Chk.
Vérif. Proc. / Design Chk
Références / Model / Proto
Vérif. Proc. / Prod. Chk
Appr. / Appd.
Date: 980722
Brut Plan No / Blank Drwg
Proto. Plan No / Proto. Drwg: BE15197
Piece/Part No: 570.39
Plan No / Drg.: 615 570393 0
Sheet 1 / 1

ANALOG DEVICES

Dual Low Offset, Low Power Operational Amplifier

OP200

FEATURES

- **Low Input Offset Voltage: 75 μV Max**
- **Low Offset Voltage Drift, Over −55°C ≤ T_A ≤ +125°C: 0.5 μV/°C Max**
- **Low Supply Current (Per Amplifier): 725 μA Max**
- **High Open-Loop Gain: 5000 V/mV Min**
- **Low Input Bias Current: 2 nA Max**
- **Low Noise Voltage Density: 11 nV/√Hz at 1 kHz**
- **Stable with Large Capacitive Loads: 10 nF Typ**
- **Pin Compatible to OP221, MC1458, and LT1013 with Improved Performance**
- **Available in Die Form**

GENERAL DESCRIPTION

The OP200 is the first monolithic dual operational amplifier to offer OP77 type precision performance. Available in the industry standard 8-pin pinout, the OP200 combines precision performance with the space and cost savings offered by a dual amplifier.

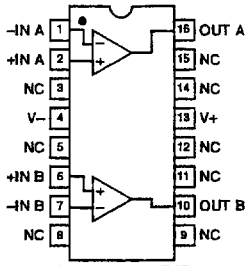
The OP200 features an extremely low input offset voltage of less than 75 μV with a drift below 0.5 μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP200 exceeds 5,000,000 into a 10 kΩ load; input bias current is under 2 nA; CMR is over 120 dB and PSRR below 1.8 μV/V. On-chip zener-zap trimming is used to achieve the extremely low input offset voltage of the OP200 and eliminates the need for offset pulling.

Power consumption of the OP200 is very low, with each amplifier drawing less than 725 μA of supply current. The total current drawn by the dual OP200 is less than one-half that of a single OP07, yet the OP200 offers significant improvements over this industry standard op amp. The voltage noise density of the OP200, 11 nV/√Hz at 1 kHz, is half that of most competitive devices.

The OP200 is pin compatible with the OP221, LM158, MC1458/1558, and LT1013.

PIN CONNECTIONS

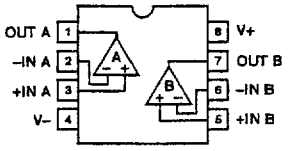
16-Pin SOIC
(S-Suffix)



NC = NO CONNECT

EPOXY MINI-DIP
(P-Suffix),

8-Pin Hermetic DIP
(Z-Suffix)



The OP200 is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the OP400.

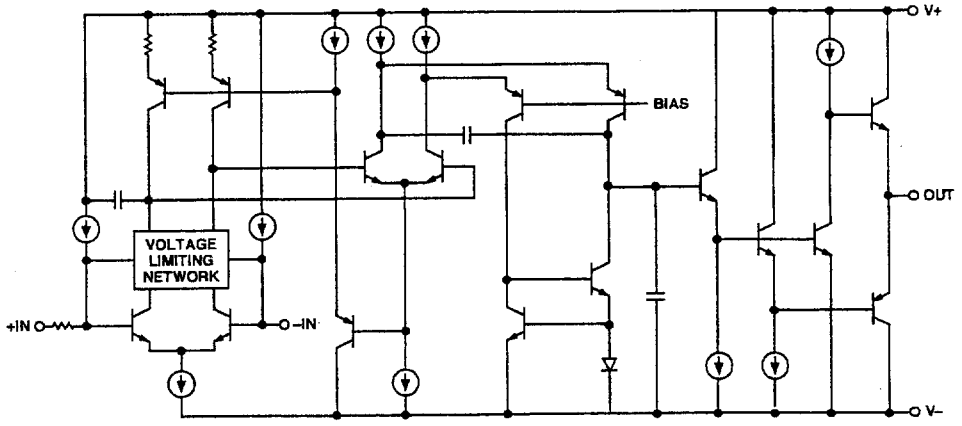


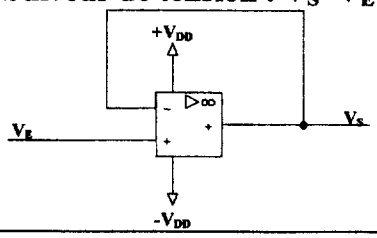
Figure 1. Simplified Schematic (One of two amplifiers is shown.)

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

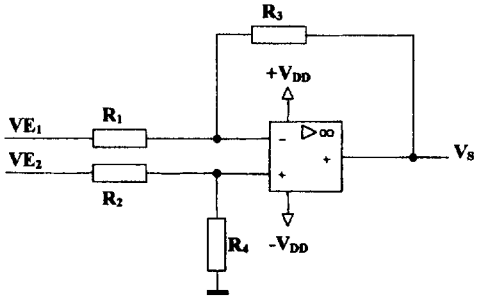
STRUCTURES DE BASE A AMPLIFICATEUR LINEAIRE INTEGRE

Suiveur de tension : $V_S=V_E$



Amplificateur de différence :

$$V_S = \frac{R_1+R_3}{R_2+R_4}\frac{R_4}{R_1} VE_2 - \frac{R_3}{R_1} VE_1$$

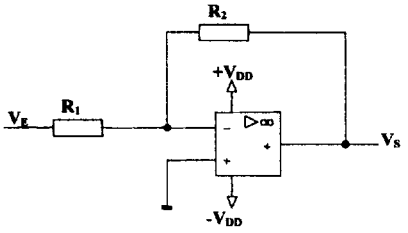


Cas particulier :

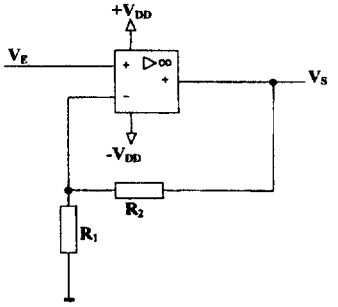
si $R_1 = R_2$ et $R_3 = R_4$ $\Rightarrow V_S = \frac{R_3}{R_1}(VE_2 - VE_1)$

si $R_1 = R_2 = R_3 = R_4$ $\Rightarrow V_S = VE_2 - VE_1$

Amplificateur inverseur : $V_S = -\frac{R_2}{R_1} V_E$

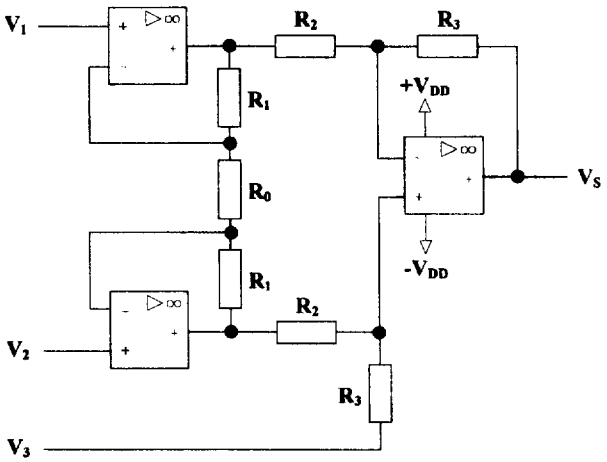


Amplificateur non-inverseur : $V_S = \left(1+\frac{R_2}{R_1}\right) V_E$



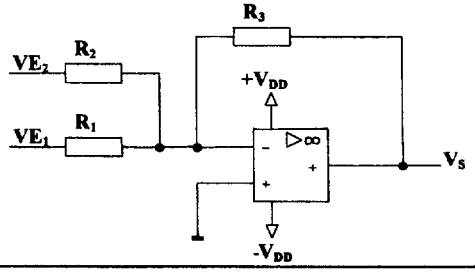
Amplificateur d'instrumentation

$$V_S = \left(1+\frac{2R_1}{R_0}\right).\frac{R_3}{R_2}(V_2 - V_1) + V_3$$



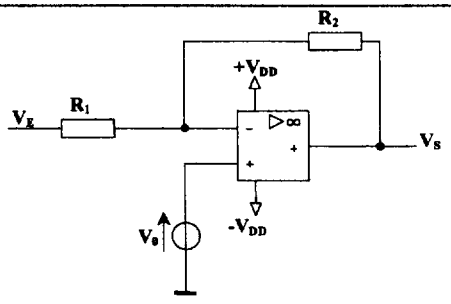
Amplificateur sommateur

$$V_S = -\left(\frac{R_3}{R_1} VE_1 + \frac{R_3}{R_2} VE_2\right)$$



Amplificateur inverseur avec décalage

$$V_S = -\frac{R_2}{R_1} V_E + \left(1+\frac{R_2}{R_1}\right) V_0$$



National Semiconductor

November 1995

MM54HC147/MM74HC147
10-to-4 Line Priority Encoder

General Description

This high speed 10-to-4 Line Priority Encoder utilizes advanced silicon-gate CMOS technology. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits. This device is fully buffered, giving it a fanout of 10 LS-TTL loads.

The MM54HC147/MM74HC147 features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.

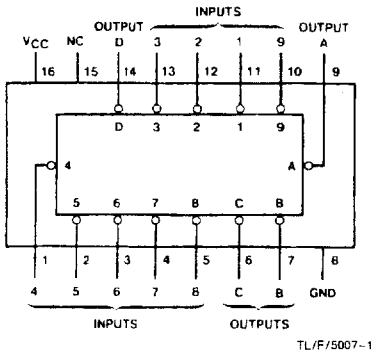
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent power consumption: 40 μW maximum at 25°C
- High speed: 31 ns propagation delay (typical)
- Low input current: 1 μA maximum
- Wide supply range: 2V to 6V

Connection and Logic Diagrams

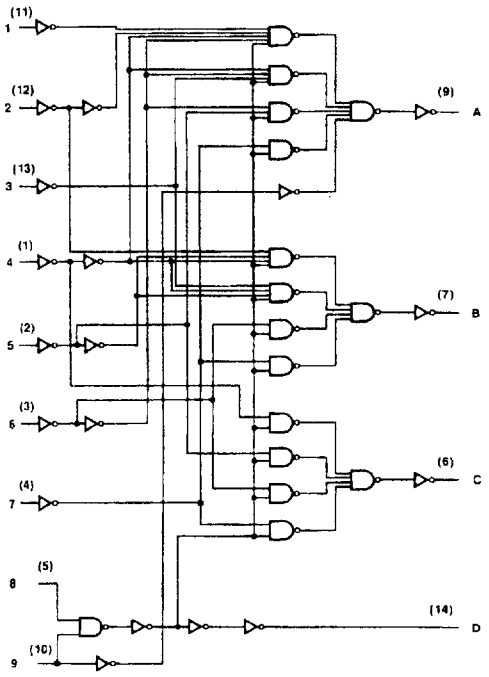
Dual-In-Line Package



TL/F/5007–1

Top View

Order Number MM54HC147 or MM74HC147



TL/F/5007–2

Truth Table

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant

RRD-B30M115/Printed in U. S. A.

MM54HC147/MM74HC147 10-to-4 Line Priority Encoder

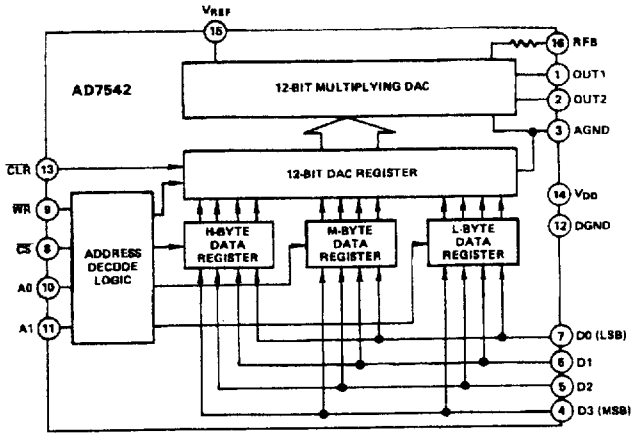
ANALOG DEVICES

CMOS µP-Compatible 12-Bit DAC

AD7542

FEATURES
Resolution: 12 Bits
Nonlinearity: ±1/2LSB T_{min} to T_{max}
Low Gain Drift: 2ppm/°C typ, 5ppm/°C max
Microprocessor Compatible
Full 4-Quadrant Multiplication
Fast Interface Timing
Low Power Dissipation: 40mW max
Low Cost
Small Size: 16-pin DIP and 20-Terminal Surface Mount Package
Latch Free (Protection Schottky Not Required)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

The functional diagram shows the AD7542 to consist of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A clear input allows the DAC register to be easily reset to all zeros when powering up the device.

The AD7542 is manufactured using an advanced thin-film on monolithic CMOS fabrication process. Multiplying capability, low power dissipation, +5V operation, small size (16-pin DIP and 20 terminal surface mount packages) and easy µP interface make the AD7542 ideal for many instrumentation, industrial control and avionics applications.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD7542—SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = −40°C to +85°C	Limit At[1] T_A = −55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
J, A, S Versions	±1	±1	±1	LSB max	
K, B, T Versions	±1/2	±1/2	±1/2	LSB max	
GK, GB, GT Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
J, A, S Versions	±1	±1	±1	LSB max	All grades are guaranteed monotonic
K, B, T Versions	±1	±1	±1	LSB max	T_{min} to T_{max}
GK, GB, GT Versions	±1	±1	±1	LSB max	
Gain Error[2]					
J, K, A, B, S, T	±3	±4	±4	LSB max	Using internal R_{FB} only (gain error can be
GK, GB, GT	±1	±1	±2	LSB max	trimmed to zero using circuits of Figure 4 & 5)
Gain Temperature Coefficient					
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection					
ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1}	10	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2}	10	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	μs max	To 1/2LSB, OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	DAC register loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	DAC register loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+2.4	+2.4	+2.4	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (See Figures 4 and 5). Data is Loaded into Data Registers in 4-Bit Bytes.				
SWITCHING CHARACTERISTICS[5]	(See Figure 1)				
t_{WR}	80	120	160	ns min	t_{WR}: WRITE pulse width
t_{AWH}	0	10	10	ns min	t_{AWH}: Address-to-WRITE hold time
t_{CWH}	0	10	10	ns min	t_{CWH}: Chip select-to-WRITE hold time
t_{CLR}	200	200	250	ns min	t_{CLR}: Minimum CLEAR pulse width
t_{CWS}	10	20	20	ns min	t_{CWS}: Chip select-to-WRITE setup time
t_{AWS}	40	40	40	ns min	t_{AWS}: Address valid-to-WRITE setup time
t_{DS}	60	100	100	ns min	t_{DS}: Data setup time
t_{DH}	10	10	10	ns min	t_{DH}: Data hold time
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	±5% for specified performance
I_{DD} (Supply Current)	2.5	2.5	2.5	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES
[1]Temperature Ranges as follows: J, K, GK Versions; −40°C to +85°C
A, B, GB Versions; −40°C to +85°C
S, T, GT Versions; −55°C to +125°C
[2]See definitions on next page.
[3]Guaranteed but not tested.
[4]Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
[5]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

AD7542

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to GND	−0.3V, V_{DD} +0.3V
V_{OUT1}, V_{OUT2} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	±25V
V_{RFB} to AGND	±25V
Power Dissipation (Package)	
Plastic	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, GK Versions)	−40°C to +85°C
Industrial (A, B, GB Versions)	−40°C to +85°C
Extended (S, T, GT Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*COMMENTS: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Gain Error	Package Option[2]
AD7542JN	−40°C to +85°C	±1LSB	±3LSB	N-16
AD7542KN	−40°C to +85°C	±1/2LSB	±3LSB	N-16
AD7542GKN	−40°C to +85°C	±1/2LSB	±1LSB	N-16
AD7542JP	−40°C to +85°C	±1LSB	±3LSB	P-20A
AD7542KP	−40°C to +85°C	±1/2LSB	±3LSB	P-20A
AD7542GKP	−40°C to +85°C	±1/2LSB	±1LSB	P-20A
AD7542AQ	−40°C to +85°C	±1LSB	±3LSB	Q-16
AD7542BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-16
AD7542GBQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-16
AD7542SQ	−55°C to +125°C	±1LSB	±3LSB	Q-16
AD7542TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-16
AD7542GTQ	−55°C to +125°C	±1/2LSB	±1LSB	Q-16
AD7542SE	−55°C to +125°C	±1LSB	±3LSB	E-20A
AD7542TE	−55°C to +125°C	±1/2LSB	±3LSB	E-20A
AD7542GTE	−55°C to +125°C	±1/2LSB	±1LSB	E-20A

NOTES
[1]To order MIL-STD-883 Class B processed parts, add /883B to part number.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

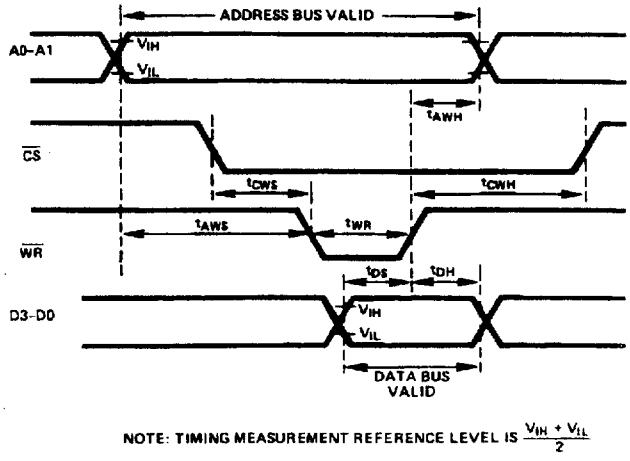
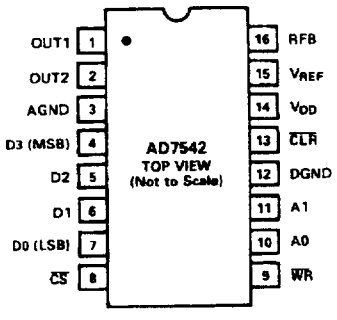


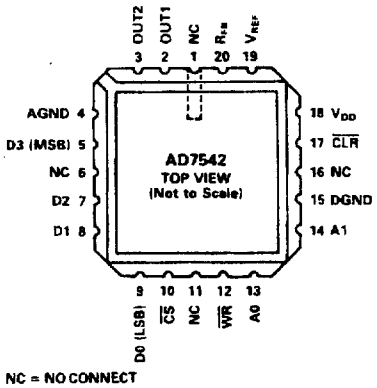
Figure 1. AD7542 Timing Diagram

PIN CONFIGURATIONS

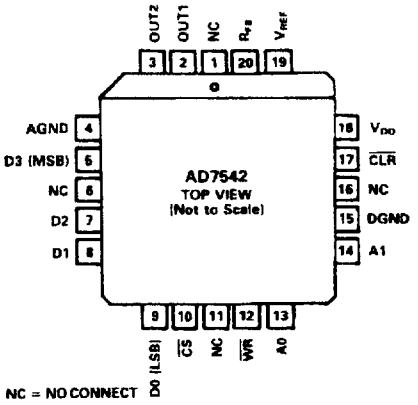
DIP



LCCC



PLCC



REV. A

AD7542

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR
Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7542 would exhibit a gain of -4095/4096. Gain error is adjustable using external trims as shown in Figures 4 and 5.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with the DAC register loaded to all 0s or at OUT2 with the DAC register loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

Table I. Pin Function Description (DIP Pin Numbers)

PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at ground
3	AGND	Analog Ground
4	D3	Data Input (MSB)
5	D2	Data Input
6	D1	Data Input
7	D0	Data Input (LSB)
8	$\overline{CS}$	Chip Select Input
9	$\overline{WR}$	WRITE Input
10	A0	Address Bus Input
11	A1	Address Bus Input
12	DGND	Digital Ground
13	$\overline{CLR}$	Clear Input
14	V_{DD}	+5V Supply Input
15	V_{REF}	Reference Input
16	R_{FB}	DAC Feedback Resistor

Analog Circuit Description

GENERAL CIRCUIT INFORMATION
The AD7542, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 2. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

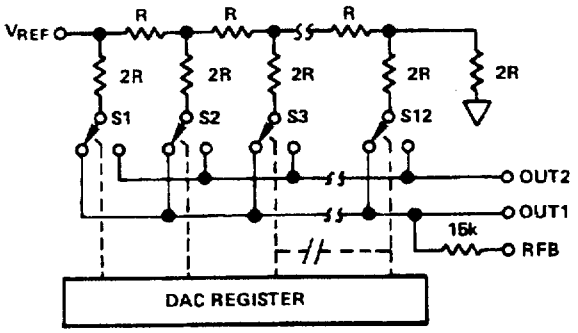


Figure 2. D/A Simplified Circuit Diagram

One of the current switches is shown in Figure 3. The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient R_{FB} is recommended to define scale factor.)

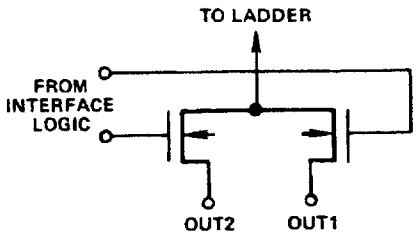


Figure 3. N-Channel Current Steering Switch

Applying the AD7542

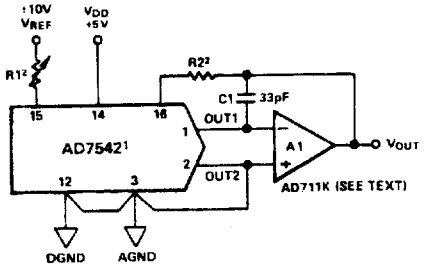
UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at V_{REF}, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 33pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD711K is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.



NOTES
1. LOGIC INPUTS OMITTED FOR CLARITY. DIP PIN NUMBERS SHOWN.
2. SEE APPLICATION HINT NO. 4

Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

Table II. Unipolar Binary Code Table for Circuit of Figure 4

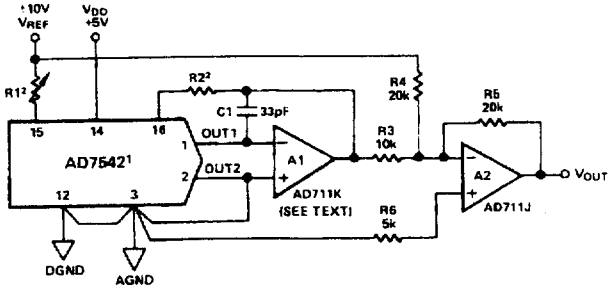
BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the circuit provides full 4-quadrant multiplication.

With the DAC register loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.



NOTES
1. LOGIC INPUTS OMITTED FOR CLARITY. DIP PIN NUMBERS SHOWN.
2. SEE APPLICATION HINT NO. 4.

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

National Semiconductor

June 1992

CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

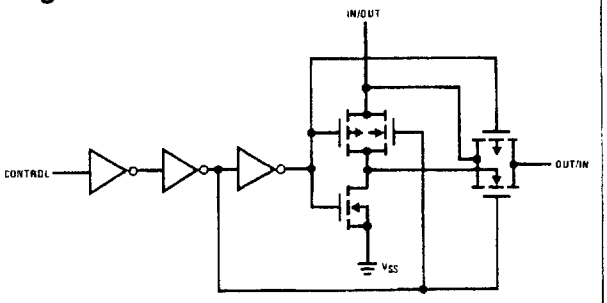
Features

- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Wide range of digital and analog switching ±7.5 V_{PEAK}
- "ON" resistance for 15V operation 80Ω
- Matched "ON" resistance over 15V signal input ΔR_{ON} = 5Ω (typ.)
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio 65 dB (typ.) @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree linearity 0.1% distortion (typ.) @ f_{is} = 1 kHz, V_{is} = $5V_{p-p}$, $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage 0.1 nA (typ.) @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance 10^{12}Ω (typ.)
- Low crosstalk between switches −50 dB (typ.) @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" 40 MHz (typ.)

Applications

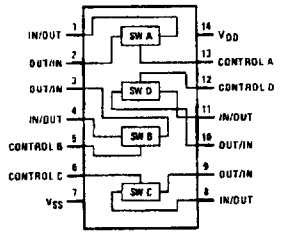
- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

Schematic and Connection Diagrams



Order Number CD4066B

Dual-In-Line Package



TL/F/5665–1

Top View

RRD-B30M105/Printed in U. S. A.