Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

DC Electrical Characteristics CD4066BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.01	0.5		15	μA
		V_{DD} = 15V		1.0		0.01	1.0		30	μA
SIGNAL INPUTS AND OUTPUTS										
R_{ON}	"ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$, $V_C = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		V_{DD} = 5V		800		270	1050		1300	Ω
		V_{DD} = 10V		310		120	400		550	Ω
		V_{DD} = 15V		200		80	240		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$, $V_C = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		V_{DD} = 10V				10				Ω
		V_{DD} = 15V				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	V_C = 0, V_{IS} = 15V and 0V, V_{OS} = 0V and 15V		±50		±0.1	±50		±500	nA
CONTROL INPUTS										
V_{ILC}	Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD}, $V_{OS} = V_{DD}$ and V_{SS}, I_{IS} = ±10 μA								
		V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V (see note 6)	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD} - V_{SS}$ = 15V, $V_{DD} \geq V_{IS} \geq V_{SS}$, $V_{DD} \geq V_C \geq V_{SS}$		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA

DC Electrical Characteristics CD4066BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		7.5	μA
		V_{DD} = 10V		2.0		0.01	2.0		15	μA
		V_{DD} = 15V		4.0		0.01	4.0		30	μA

MAXIM

Calibrated 12-Bit A/D Converter

MX7578

General Description

The MX7578 is a complete, calibrated 12-bit A/D converter (ADC) which includes a conversion clock. Internal calibration circuitry maintains true 12-bit performance over the full operating temperature range without external adjustments. In addition, each conversion includes an auto-zero cycle which reduces zero errors to typically below 100µV.

CHIP SELECT, READ, and WRITE inputs are included for easy microprocessor interfacing without additional logic. 2-byte, 12-bit conversion data is provided over an 8-bit three-state output bus. Either byte may be read first. Two converter busy flags facilitate polling of the converter's status.

The MX7578's analog input range is 0V to +5V when using a +5V reference. Refer to Maxim's MAX178 data sheet for a plug-in upgrade with track/hold and internal reference.

Applications

Digital-Signal Processing
Audio and Telecom Processing
High-Speed Data Acquisition
High-Accuracy Process Control

Features

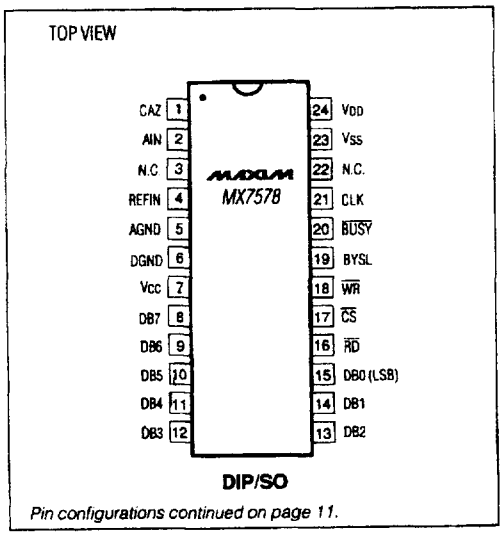
- ♦ **Continuous Transparent Calibration of Offset and Gain**
- ♦ **True 12-Bit Performance without Adjustments**
- ♦ **Zero Error Typically <100µV**
- ♦ **Standard Microprocessor Interface**
- ♦ **24-Pin DIP/Wide SO and 28-Pin PLCC Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MX7578KN	0°C to +70°C	24 Plastic DIP
MX7578KCWG	0°C to +70°C	24 Wide SO**
MX7578KP	0°C to +70°C	28 PLCC
MX7578K/D	0°C to +70°C	Dice**
MX7578KEWG	-40°C to +85°C	24 Wide SO**
MX7578BQ	-40°C to +85°C	24 CERDIP*
MX7578BD	-40°C to +85°C	24 Ceramic SB
MX7578TQ	-55°C to +125°C	24 CERDIP*
MX7578TD	-55°C to +125°C	24 Ceramic SB

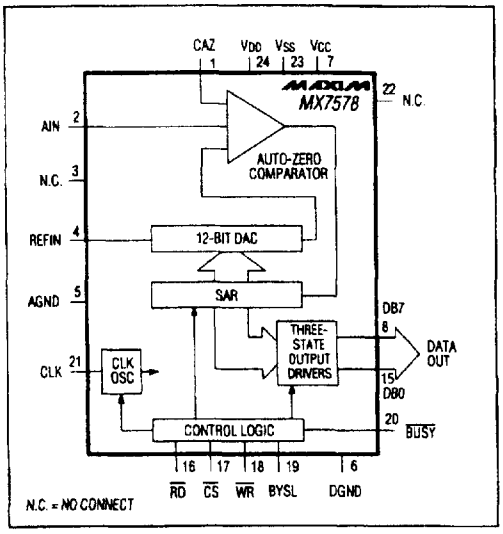
* *Maxim reserves the right to ship Ceramic SB in lieu of CERDIP packages.*
** *Consult factory.*

Pin Configurations



Pin configurations continued on page 11.

Functional Diagram



LM393, LM293, LM2903, LM2903V, NCV2903

Low Offset Voltage Dual Comparators

The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range−to−ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer, automotive, and industrial electronics.

- Wide Single−Supply Range: 2.0 Vdc to 36 Vdc
- Split−Supply Range: ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance

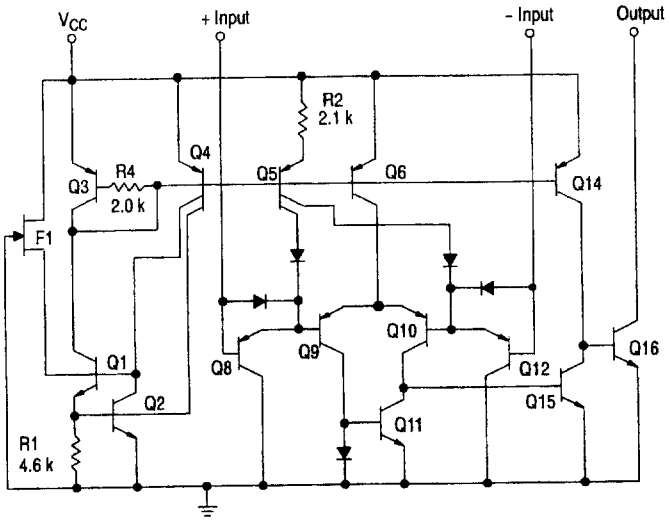
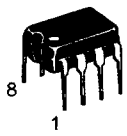


Figure 1. Representative Schematic Diagram
(Diagram shown is for 1 comparator)

ON Semiconductor

http://onsemi.com

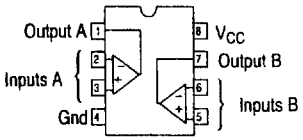


PDIP−8
N SUFFIX
CASE 626

SO−8
D SUFFIX
CASE 751

Micro8™
DM SUFFIX
CASE 846A

PIN CONNECTIONS



(Top View)

ORDERING & DEVICE MARKING INFORMATION

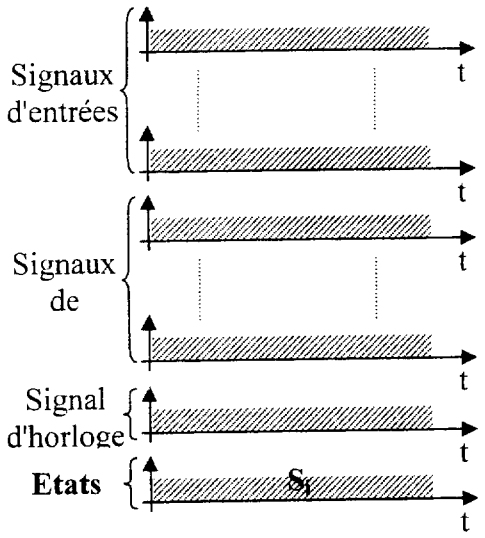
See detailed ordering and shipping information and marking information in the package dimensions section on page 6 of this data sheet.

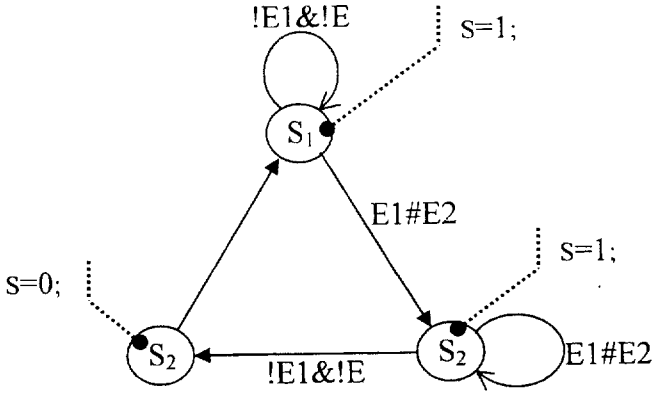
September, 2003 − Rev. 11

Publication Order Number:
LM393/D

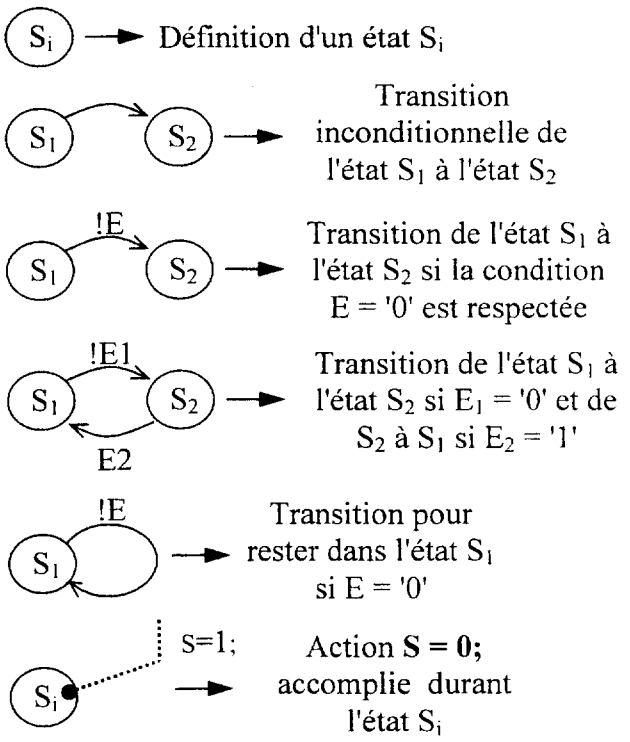
PRINCIPES DE CONSTRUCTION D'UN DIAGRAMME D'ETATS.

Chronogrammes décrivant la fonction





Règles de construction



Remarques :

Les transitions ont lieu à chaque front actif de l'horloge.

Une transition doit toujours être possible.

Les actions sont exprimées en ABEL pour permettre la synthèse automatique du diagramme d'états.

Syntaxe ABEL :

! pour le complément,
& opérateur logique ET,
opérateur logique OU,
$ opérateur logique OU exclusif,
!$ opérateur logique OU exclusif complémenté,
; la fin d'une équation se traduit par le caractère point virgule,
<= inférieure ou égale,
>= supérieure ou égale,
^b, ^o, ^d, ^h précise la base numérique **b**inaire, **o**ctale, **d**écimale et **h**exadécimale.

Order this document
by MC6840/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC6840

Programmable Timer Module (PTM)

The MC6840 is a programmable subsystem component of the M6800 Family designed to provide variable system time intervals.

The MC6840 has three 16-bit binary counters, three corresponding control registers, and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The MC6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring, and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

- Operates from a Single 5-Volt Power Supply
- Fully TTL Compatible
- Single System Clock Required (Enable)
- Selectable Prescaler on Timer 3 Capable of 4 MHz for the MC6840, 6 MHz for the MC68A40 and 8 MHz for the MC68B40
- Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- Readable Down Counter Indicates Counts to Go Until Time-Out
- Selectable Gating for Frequency or Pulse-Width Comparison
- $\overline{RESET}$ Input
- Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- Three Maskable Outputs

MOTOROLA
DS9802R3

Valeurs normalisées de résistances

Caractéristiques des principales séries de valeurs normalisées :

Série	E3	E6	E12	E24	E48	E96	E192
Nombre de valeurs	3	6	12	24	48	96	192
Tolérance	± 30 %	± 20 %	± 10 %	± 5 %	± 2 %	± 1 %	± 0,5 % ± 0,1 % ± 0,01 %

Valeurs de la série normalisée E24 :

110	120	130	150	160	180	200	220	240	270	300	330
360	390	430	470	510	560	620	680	750	820	910	1000

CYPRESS

PALCE16V8

Flash Erasable, Reprogrammable CMOS PAL® Device

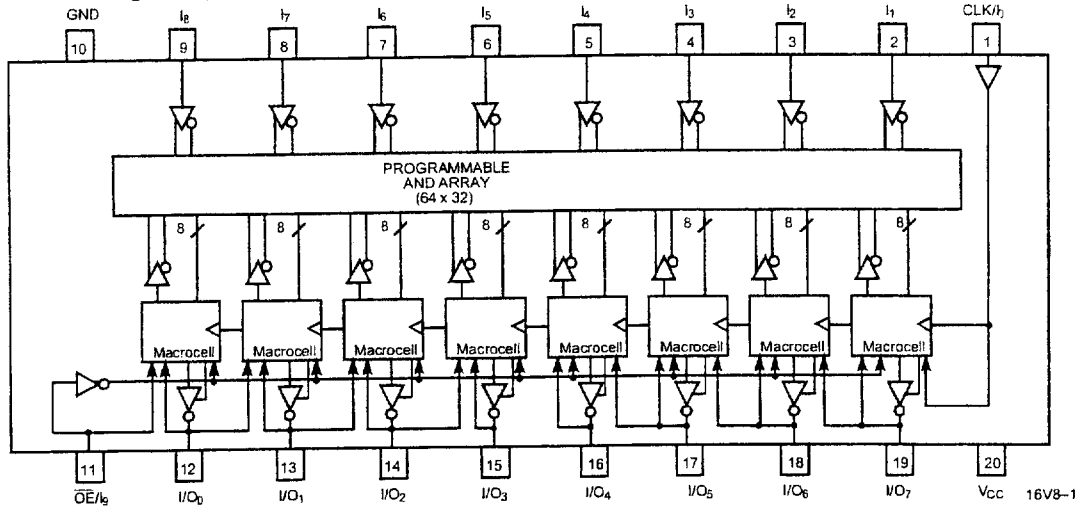
Features

- Active pull-up on data input pins
- Low power version (16V8L)
  - 55 mA max. commercial (10, 15, 25 ns)
  - 65 mA max. industrial (10, 15, 25 ns)
  - 65 mA military (15 and 25 ns)
- Standard version has low power
  - 90 mA max. commercial (10, 15, 25 ns)
  - 115 mA max. commercial (7 ns)
  - 130 mA max. military/industrial (10, 15, 25 ns)
- CMOS Flash technology for electrical erasability and reprogrammability
- PCI compliant
- User-programmable macrocell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
- Up to 16 input terms and 8 outputs
- 7.5 ns com'l version
  5 ns t_{CO}
  5 ns t_S
  7.5 ns t_{PD}
  125-MHz state machine
- 10 ns military/industrial versions
  7 ns t_{CO}
  10 ns t_S
  10 ns t_{PD}
  62-MHz state machine
- High reliability
  - Proven Flash technology
  - 100% programming and functional testing

Functional Description

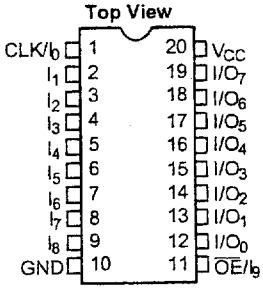
The Cypress PALCE16V8 is a CMOS Flash Electrical Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-product (AND-OR) logic structure and the programmable macrocell.

Logic Block Diagram (PDIP/CDIP)

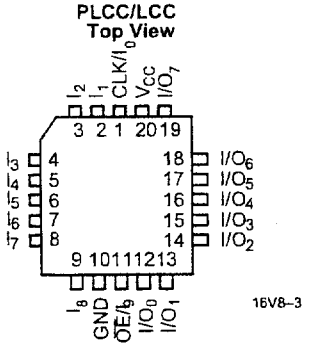


Pin Configurations

DIP
Top View



PLCC/LCC
Top View



Cypress Semiconductor Corporation • 3901 North First Street • San Jose • CA 95134 • 408-943-2600
September 3, 1998

CYPRESS

PALCE20V8

Flash Erasable, Reprogrammable CMOS PAL® Device

Features

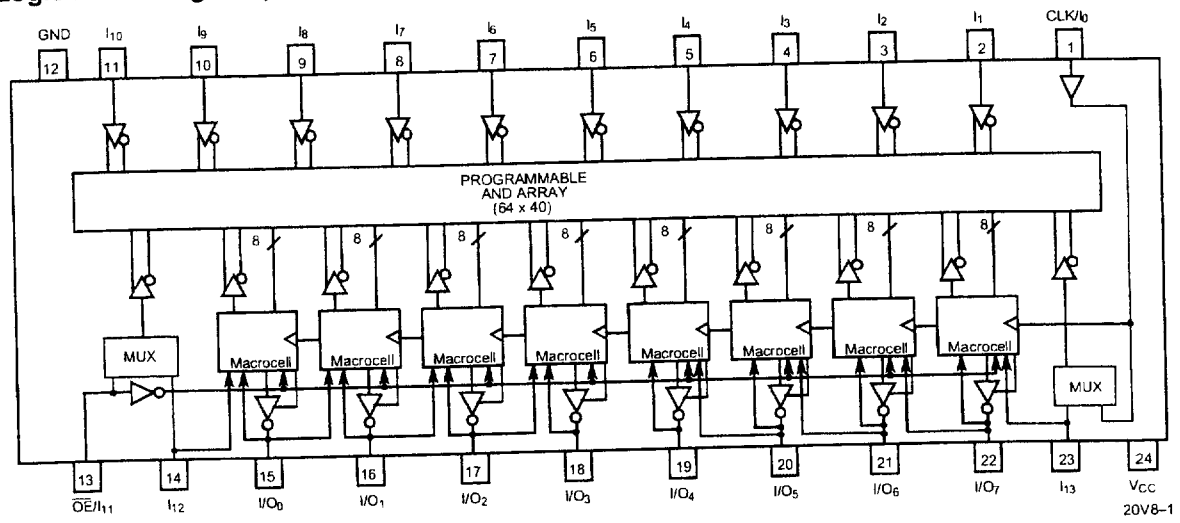
- Active pull-up on data input pins
- Low power version (20V8L)
  - 55 mA max. commercial (15, 25 ns)
  - 65 mA max. military/industrial (15, 25 ns)
- Standard version has low power
  - 90 mA max. commercial (15, 25 ns)
  - 115 mA max. commercial (10 ns)
  - 130 mA max. military/industrial (15, 25 ns)
- CMOS Flash technology for electrical erasability and reprogrammability
- User-programmable macrocell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
- QSOP package available
  - 10, 15, and 25 ns com'l version
  - 15, and 25 ns military/industrial versions
- High reliability
  - Proven Flash technology
  - 100% programming and functional testing

Functional Description

The Cypress PALCE20V8 is a CMOS Flash Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-product (AND-OR) logic structure and the programmable macrocell.

The PALCE20V8 is executed in a 24-pin 300-mil molded DIP, a 300-mil cerdip, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and a 24-lead quarter size outline. The device provides up to 20 inputs and 8 outputs. The PALCE20V8 can be electrically erased and reprogrammed. The programmable macrocell enables the device to function as a superset to the familiar 24-pin PLDs such as 20L8, 20R8, 20R6, 20R4.

Logic Block Diagram (PDIP/CDIP/QSOP)



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June 1994 - Revised March 26, 1997

CYPRESS

PALCE22V10

Flash Erasable, Reprogrammable CMOS PAL® Device

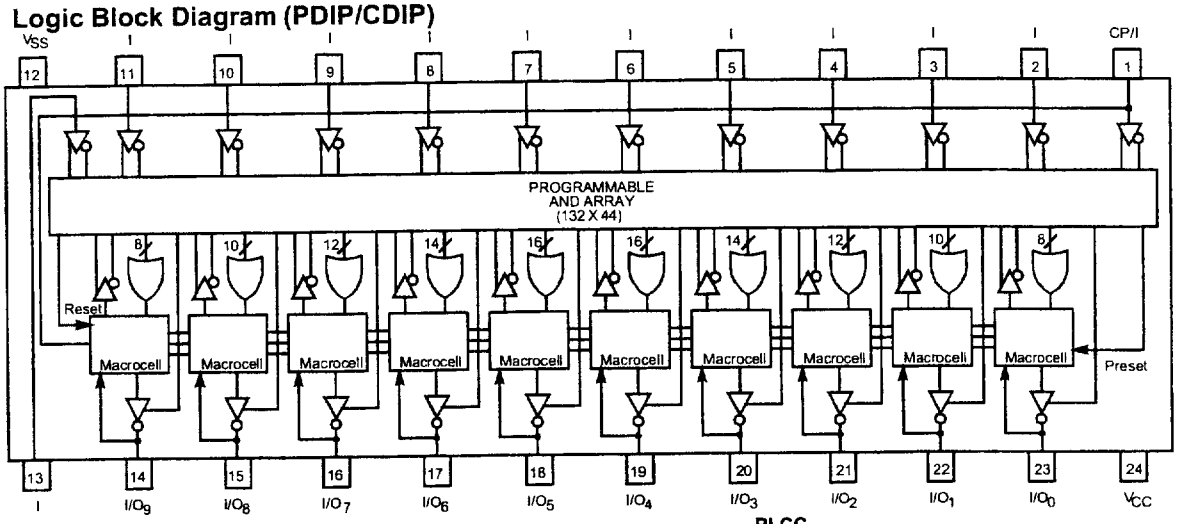
Features

- Low power
  - 90 mA max. commercial (10 ns)
  - 130 mA max. commercial (5 ns)
- CMOS Flash EPROM technology for electrical erasability and reprogrammability
- Variable product terms
  - 2 x (8 through 16) product terms
- User-programmable macrocell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
- Up to 22 input terms and 10 outputs
- DIP, LCC, and PLCC available
  - 5 ns commercial version
    4 ns t_{CO}
    3 ns t_S
    5 ns t_{PD}
    181-MHz state machine
  - 10 ns military and industrial versions
    7 ns t_{CO}
    6 ns t_S
    10 ns t_{PD}
    110-MHz state machine
  - 15-ns commercial, industrial, and military versions
  - 25-ns commercial, industrial, and military versions
- High reliability
  - Proven Flash EPROM technology
  - 100% programming and functional testing

Functional Description

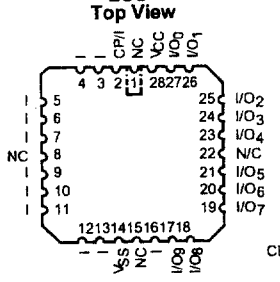
The Cypress PALCE22V10 is a CMOS Flash Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and the programmable macrocell.

Logic Block Diagram (PDIP/CDIP)



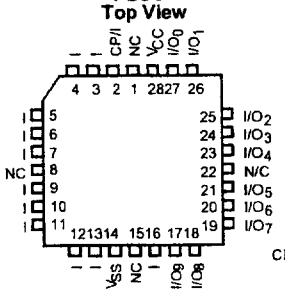
Pin Configuration

LCC Top View



CE22V10-2

PLCC Top View



CE22V10-3

CE22V10-1

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September 1996

CYPRESS

CY7C372i

UltraLogic™ 64-Macrocell Flash CPLD

Features

- **64 macrocells in four logic blocks**
- **32 I/O pins**
- **5 dedicated inputs including 2 clock pins**
- **In-System Reprogrammable (ISR™) Flash technology**
  - **JTAG interface**
- **Bus Hold capabilities on all I/Os and dedicated inputs**
- **No hidden delays**
- **High speed**
  - f_{MAX} = 125 MHz
  - t_{PD} = 10 ns
  - t_S = 5.5 ns
  - t_{CO} = 6.5 ns
- **Fully PCI compliant**
- **3.3V or 5.0V I/O operation**
- **Available in 44-pin PLCC, TQFP, and CLCC packages**
- **Pin compatible with the CY7C371i**

Functional Description

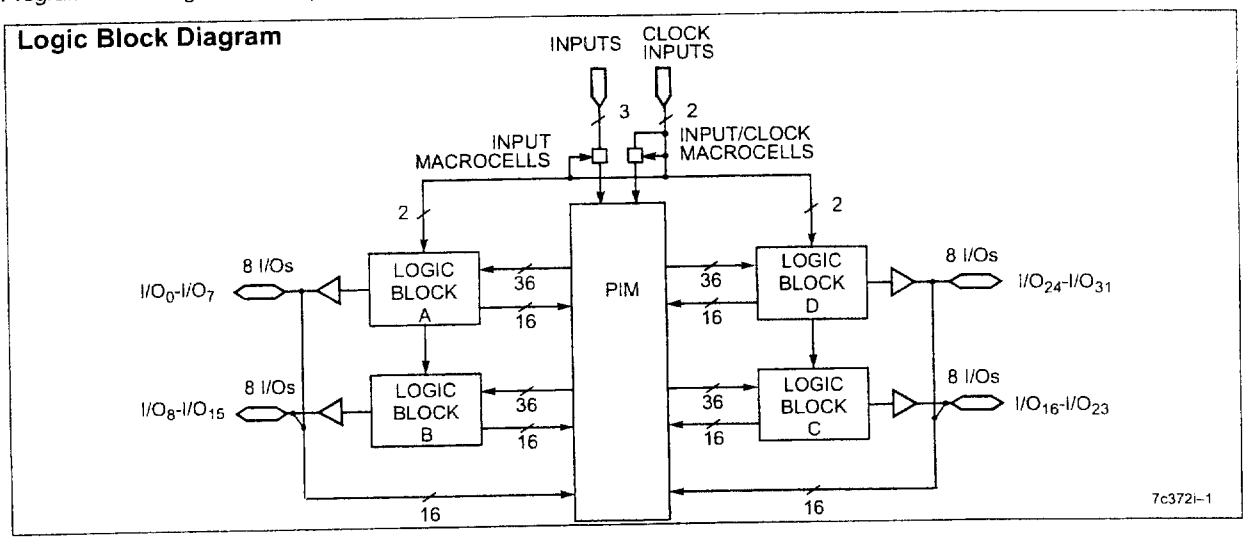
The CY7C372i is an In-System Reprogrammable Complex Programmable Logic Device (CPLD) and is part of the FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C372i is designed to bring the ease of use and high performance of the 22V10, as well as PCI Local Bus Specification support, to high-density CPLDs.

Like all of the UltraLogic™ FLASH370i devices, the CY7C372i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The Cypress ISR function is implemented through a JTAG serial interface. Data is shifted in and out through the SDI and SDO pins. The ISR interface is enabled using the programming voltage pin (ISR_{EN}). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 64 macrocells in the CY7C372i are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Logic Block Diagram



Selection Guide

	7C372i-125	7C372i-100	7C372i-83	7C372iL-83	7C372i-66	7C372iL-66
Maximum Propagation Delay[1], t_{PD} (ns)	10	12	15	15	20	20
Minimum Set-up, t_S (ns)	5.5	6.0	8	8	10	10
Maximum Clock to Output[1], t_{CO} (ns)	6.5	6.5	8	8	10	10
Typical Supply Current, I_{CC} (mA)	75	75	75	45	75	45

Note:
1. The 3.3V I/O mode timing adder, $t_{3.3IO}$, must be added to this specification when V_{CCIO} = 3.3V.

Cypress Semiconductor Corporation • 3901 North First Street • San Jose • CA 95134 • 408-943-2600
Document #: 38-03033 Rev. ** Revised July 10, 2000

CYPRESS

CY7C374i

UltraLogic™ 128-Macrocell Flash CPLD

Features

- 128 macrocells in eight logic blocks
- 64 I/O pins
- 5 dedicated inputs including 4 clock pins
- In-System Reprogrammable™ (ISR™) Flash technology
  - —JTAG interface
- Bus Hold capabilities on all I/Os and dedicated inputs
- No hidden delays
- High speed
  - —f_{MAX} = 125 MHz
  - —t_{PD} = 10 ns
  - —t_S = 5.5 ns
  - —t_{CO} = 6.5 ns
- Fully PCI compliant
- 3.3V or 5.0V I/O operation
- Available in 84-pin PLCC, 84-pin CLCC, and 100-pin TQFP packages
- Pin compatible with the CY7C373i

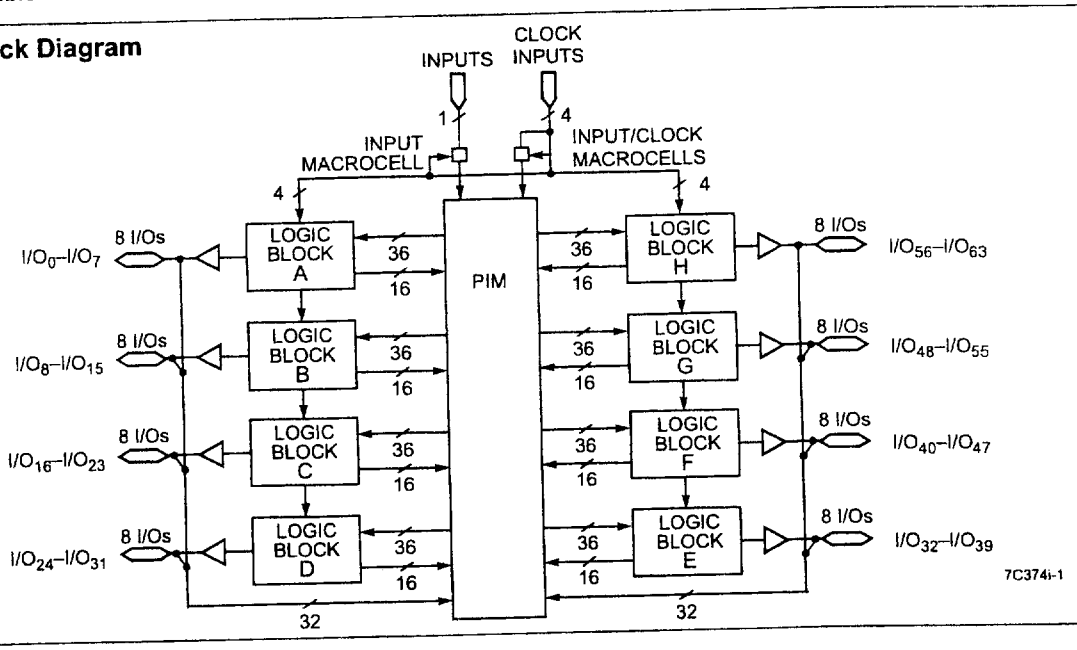
Functional Description

The CY7C374i is an In-System Reprogrammable Complex Programmable Logic Device (CPLD) and is part of the FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C374i is designed to bring the ease of use as well as PCI Local Bus Specification support and high performance of the 22V10 to high-density CPLDs.

Like all of the UltraLogic™ FLASH370i devices, the CY7C374i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The Cypress ISR function is implemented through a JTAG serial interface. Data is shifted in and out through the SDI and SDO pin. The ISR interface is enabled using the programming voltage pin (ISR_{EN}). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 128 macrocells in the CY7C374i are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

Logic Block Diagram



Selection Guide

	7C374i–125	7C374i–100	7C374i–83	7C7374iL–83	7C374i–66	7C374iL–66
Maximum Propagation Delay[1], t_{PD} (ns)	10	12	15	15	20	20
Minimum Set-Up, t_S (ns)	5.5	6	8	8	10	10
Maximum Clock to Output[1], t_{CO} (ns)	6.5	7	8	8	10	10
Typical Supply Current, I_{CC} (mA)	125	125	125	75	125	75

Note:
1. The 3.3V I/O mode timing adder, $t_{3.3IO}$, must be added to this specification when V_{CCIO} = 3.3V.

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