Ethernet TCP/IP - Protocole Modbus TCP
Analyse de trame : Requête (Query)

■ **Couche Application : Données = Protocole Modbus**

Préfixe :
Identificateur de transaction : 0x0000
Identificateur de protocole : 0x0000 = Modbus
Longueur : 0x0006

```
00 00 54 10  07 ED 00 06  29 15 3A 83  08 00 45 00
00 34 76 01  40 00 80 06  10 AF 8B A0  AE 6D 8B A0
AE 65 04 18  01 F6 00 24  0B FD 17 5E  6C E9 50 18
21 21 84 0B  00 00 00 00  00 00 00 06  00 03 00 00
00 01
```

Unit Identifier :
0x00

Ethernet TCP/IP - Protocole Modbus TCP
Analyse de trame : Requête (Query)

■ **Couche Application : Données = Protocole Modbus**

Code Fonction :
0x03 = Lecture registres

Numéro du premier mot à lire:
0x0000 = %MW0

```
00 00 54 10  07 ED 00 06  29 15 3A 83  08 00 45 00
00 34 76 01  40 00 80 06  10 AF 8B A0  AE 6D 8B A0
AE 65 04 18  01 F6 00 24  0B FD 17 5E  6C E9 50 18
21 21 84 0B  00 00 00 00  00 00 00 06  00 03 00 00
00 01
```

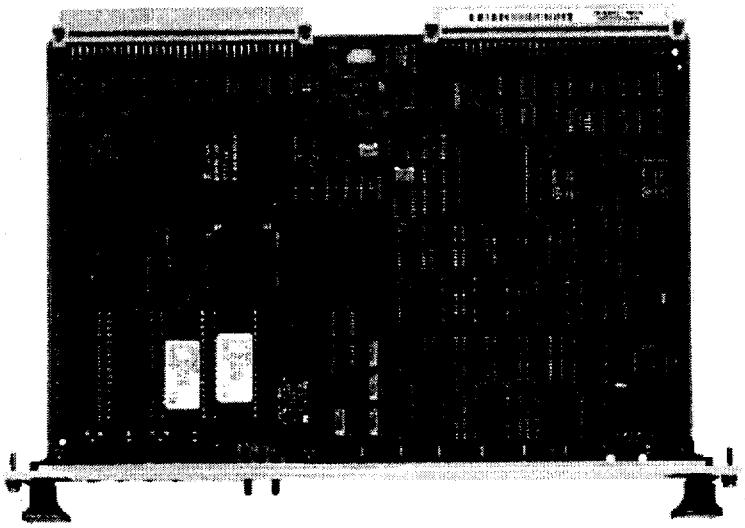
Nombre de mot à lire :
0x0001 = 1

Pour la réponse le champ indiquant« numéro du premier mot à lire »(sur deux octets) devient « nombre d'octets lus »(sur un octet) et celui « nombre de mot à lire »(sur deux octets) devient « valeur du mot lu »(sur deux octets).

Annexe 7

MOTOROLA COMPUTER GROUP
Board Level Products

MVME147
SINGLE-BOARD COMPUTER



Advantages

The MVME147 series offers one of the world's finest VMEbus single-board computers. The on-board resources and peripheral controllers eliminate the need for additional modules in the VMEbus backplane thus reducing costs and freeing up valuable bus slots for additional functions. The MVME147 series features an MC68030 enhanced 32-bit microprocessor. The MC68030 was the first general purpose microprocessor with on-chip cache memory for both instructions and data which increases the processor's efficiency by 20 to 40 percent. The MC68030 features a complete memory management unit (MMU) which provides the software protection and virtual memory functions critical to many applications.

MOTOROLA

Program and Data Address Spaces

The memory map of devices that respond in user data, user program, supervisor data, and super prog spaces is shown in the following tables. The entire map from $00000000 to $FFFFFFFF is shown in the next table. The I/O devices are further defined in Table 3-4.

Table 3-3. MC68030 Main Memory Map

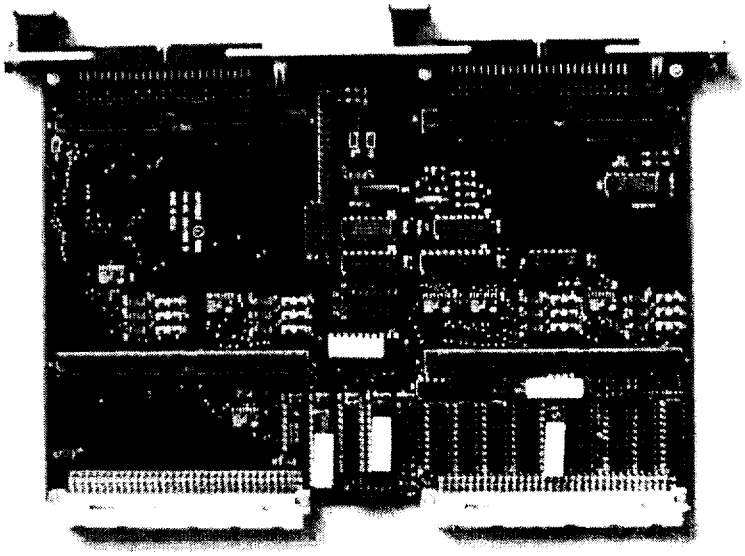
Address Range	Devices Accessed	Port Size	Size	H/W Cache Inhibit	Notes
00000000-DRAMsize	Onboard DRAM	D32	4-32MB	No	1,2
DRAMsize-EFFFFFFF	VMEbus A32/A24	D32	3GB	Yes	3,4
F0000000-F0FFFFFF	VMEbus A24	D16	16MB	Yes	
F1000000-FF7FFFFF	VMEbus A32	D16	232MB	Yes	
FF800000-FF9FFFFF	ROM/EEPROM bank 1	D16	2MB	Yes	
FFA00000-FFBFFFFF	ROM/EEPROM bank 2	D16	2MB	Yes	
FFC00000-FFFDFFFF	Reserved	N/A	4MB	Yes	3
FFFE0000-FFFE4FFF	Local I/O devices	D8/D16/D32	20KB	Yes	
FFFE5000-FFFEFFFF	Reserved	N/A	44KB	Yes	
FFFF0000-FFFFFFFF	VMEbus short I/O	D16	64KB	Yes	
Notes:					

Annexe 8

GREEN SPRING COMPUTERS

User Manual

VIPC610



Quad IndustryPack® Carrier for 6U VMEbus Systems

Product Description

The VIPC610 VMEbus IP carrier is part of the IndustryPack® family of modular I/O components. As a carrier board, the VIPC610 provides mechanical support and the electrical interfaces to four single high IndustryPacks, or two double high IPs.

Input/output, memory, and interrupt functions are supported. Battery backup is provided on board.

The VIPC610 conforms to the IndustryPack Logic Interface Specification. This guarantees compatibility with the wide range of IndustryPacks currently available and planned.

Each of the IndustryPacks interfaces with a 50-pin flat cable header accessible through the front panel of the VIPC610. The four IP positions are generally called slots, and are identified by the letters A, B, C, and D. The interfaces to the A and C packs mate with a straight receptacle connector; the interfaces to the B and D packs mate with a right angle connector. This arrangement provides for inherent strain relief. The interface connectors are mounted directly on the VME board (not on the IPs), providing a modular and reliable cabling system. Interface cable may be inserted or removed without removing the VIPC610 from the VME chassis. IPs may be snapped in or out without interfering with the I/O cabling.

IndustryPack I/O is mapped into the VMEbus A16/D16 space. Both user and supervisor accesses are supported, as are read-modify-write ("test and set") operations. The size of I/O on each IP is fixed by the IP Specification at 64 16-bit words. In addition each IP has an identification PROM which occupies 64 words. Thus the four IPs occupy 1024 bytes out of the VMEbus' 64 Kbyte "short I/O" space. The VIPC610 occupies a total of 2048 bytes in the short I/O space.

I/O Addressing

I/O addressing on the VIPC610 is determined by two elements. The first is the base address of the board. Second is the offset of the specific IP. The setting of the base address is explained below, followed by a map showing the offsets for the four IPs. Each IP has 64 16-bit words in its I/O space. Each IP also has an ID PROM that occupies another 64 words.

The VIPC610 occupies 1024 bytes in the VMEbus "short I/O," or A16/D16 space. This consists of 64 16-bit words for each IP's I/O and ID space. The board's base address is set with six shunts, or "jumpers." The location of this E3-E7 configuration block is shown in Figure 19 near the end of this manual.

An installed shunt selects a given address line as zero. A removed shunt selects the address line as a one. Thus a base address of $0000 (in A16) is created when all six shunts are installed. A base address of $FC00 (in A16) is created when all six shunts are removed. (For many host CPU boards the A16 space is accessed by beginning a 24-bit address with $FF, or a 32-bit address with $FFFF. See your CPU's User Manual for more information on address space mapping.) The relationship of shunt locations to address lines is shown in the chart below in Figure 1. E7 and E3 may be located on the board from Figure 19 near the end of this manual. Pin one of all configuration blocks is identified with a square pin, observable on the solder side of VIPC610.

The I/O base address shunts are also used to select the memory base address for the VIPC610, if memory is enabled. As an example, if the I/O base address is $6000 (in A16 space), then the memory base address is $600000 (in the A24 space). See the section following, Memory Addressing, for more information.

Shunt Location	Corresponding Address Line
E7-7 to E3-7	A15
E7-6 to E3-6	A14
E7-5 to E3-5	A13
E7-4 to E3-4	A12
E7-3 to E3-3	A11
E7-2 to E3-2	A10

Figure 1 I/O Base Address Shunt Assignment

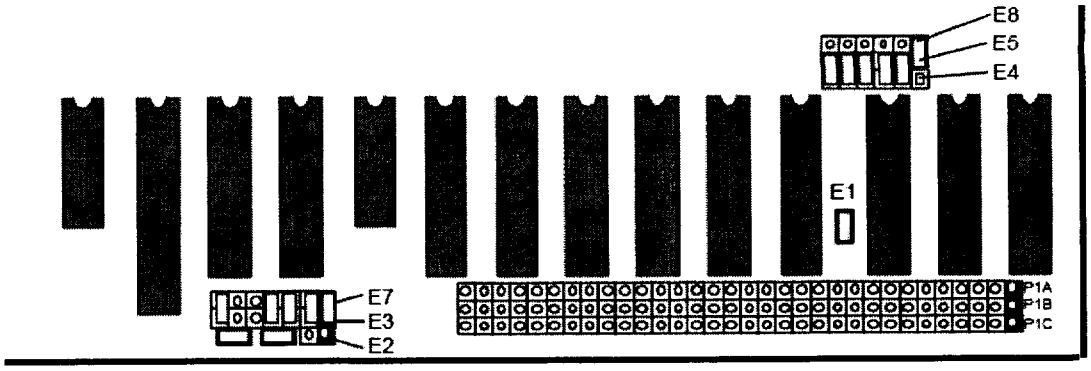


Figure 2 Default jumper setting for I/O Address of $6000.

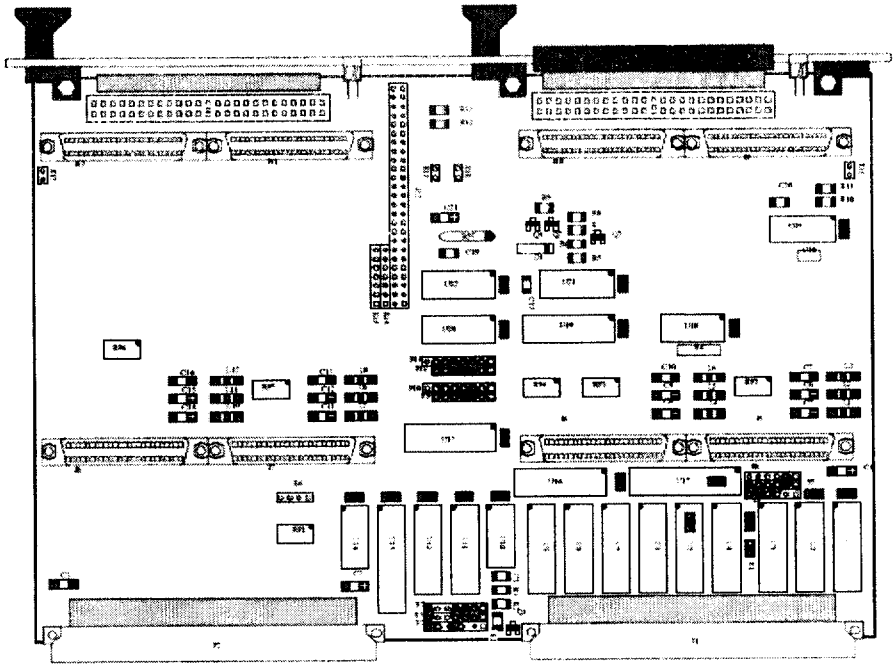
The four IP slots are addressed on the VIPC610 as shown below in Figure 3.

Address Offset	Assignment
I/O Base + $0000	IP A, I/O Space
I/O Base + $0080	IP A, ID Space
I/O Base + $0100	IP B, I/O Space
I/O Base + $0180	IP B, ID Space
I/O Base + $0200	IP C, I/O Space
I/O Base + $0280	IP C, ID Space
I/O Base + $0300	IP D, I/O Space
I/O Base + $0380	IP D, ID Space

Figure 3 : IP I/O Address Offset Assignment

Each IndustryPack has a fixed size I/O space of 64 16-bit words, which is 128 bytes ($80 bytes in hexadecimal). Many IPs use only the low order, or odd byte. In this case bytes are accessed at location offsets of $1, $3, etc. This odd byte I/O convention is a 68000 family processor and VMEbus standard. Most IPs do not use all 64 words of their allotted I/O space.

If multiple VIPC610 are used in a system they are commonly addressed in increments of $800 hex. Thus the first VIPC610 might have the factory default I/O address of $6000, the second starts at $6800, the third at $7000, etc.



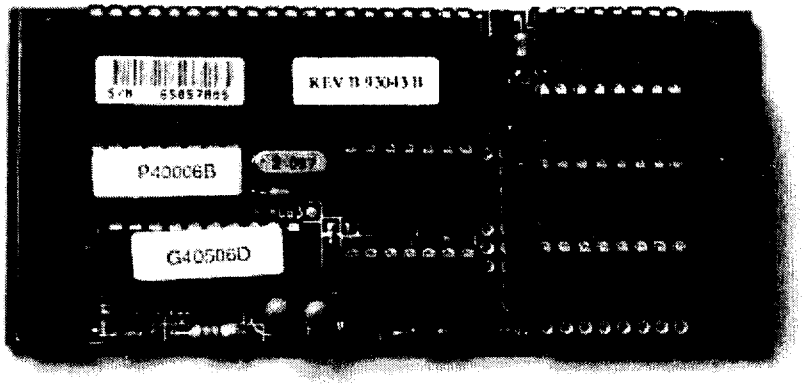
Annexe 9

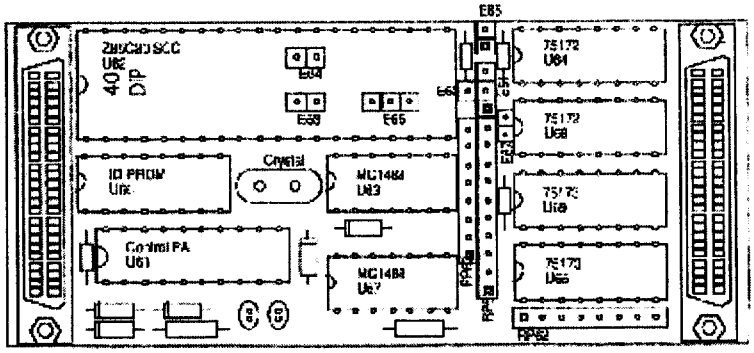
GREEN SPRING COMPUTERS

User Manual

IP-Serial

Dual Channel RS-232 / RS-422/RS-485 Multi-mode Serial Interface IndustryPack®





Product Description

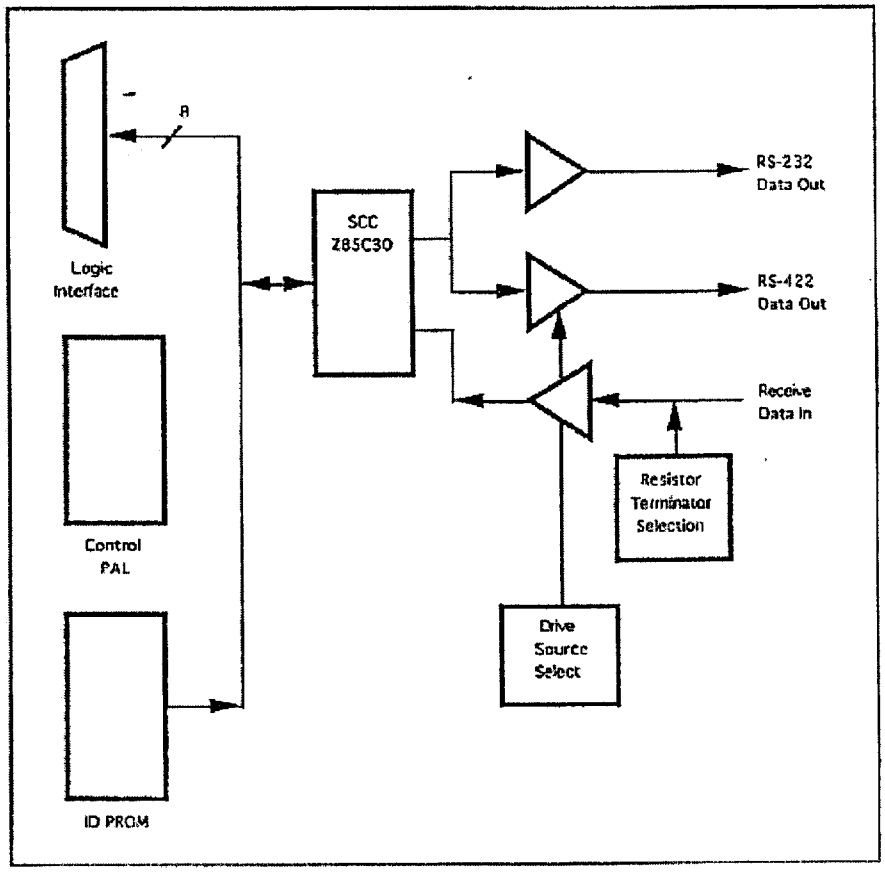
IP-Serial is part of the Industryrack® family of modular 1/0 components. It provides two channels of high performance multi-mode serial communication. RS-232-D, RS-422, and RS-485 are fully supported. (For RS-485 support, order the -485 option.)

Features include programmable baud rates to 2 Mbit/sec; asynchronous or synchronous protocols including NRZ, NRZI, FM, Tl, SDLC/HDLC.

IP-Serial supports full modem control lines, including RTS, CTS, DTR, DCD, Clock Out and Clocking.

The communications controller used is the industry standard 85C30. This controller chip includes enhanced functionality for synchronous protocols, such as loop mode, frame control, CRC-16 and CCITI generators and a 10 x 19 SDLC/HDLC Frame Status FIFO.

A block diagram of the IP-Serial is shown in Figure 1 below.



VMEbus Addressing

IP-Serial is programmed entirely through the on board Z85C30 Serial Communications Controller (SCC). Users will find both programming and applications easier if they have reference to the Z85C30 Data Sheet. This data sheet is available from Zilog Corporation or GreenSpring Computers as part of the IP-Serial Engineering Kit.

IP-Serial is a straight-forward implementation of the 85C30 SCC. The two channels, called A and B, are substantially independent. Each channel has Il read registers and 16 write registers. Registers are selected primarily by the least four bits written to write register O. This register selection process is referred to as "internal addressing."

There are four "external" addresses that are used to talk to the SCC. These select channels A or B, and data or control. These addresses are shown in Figure 2, below. Sec the next section for Nubus addressing.

All programmed communication with the SCC occurs in the IndustryPack I/O space.

Address	Function
base + 1	Channel B, Control
base + 3	Channel B, Data
base + 5	Channel A, Control
base + 7	Channel A, Data

Figure 2 : VMEbus Address Map

Annexe 10

ZILOG

SCC/ESCC

User's Manual

UM010901-0601

3.2 BAUD RATE GENERATOR

The Baud Rate Generator (BRG) is essential for asynchronous communications. Each channel in the SCC contains a programmable baud rate generator. Each generator consists of two 8-bit, time-constant registers forming a16-bit time constant, a 16-bit down counter, and a flip-flop on the output so that it outputs a square wave. On start-up, the flip-flop on the output is set High, so that it starts in a known state, the value in the time-constant register is loaded into the counter, and the counter begins counting down. When a count of zero is reached, the output of the baud rate generator toggles, the value in the time-constant register is loaded into the counter, and the process starts over. The programmed time constant is read from RR12 and RR13. A block diagram of the baud rate generator is shown in Figure 3-1.

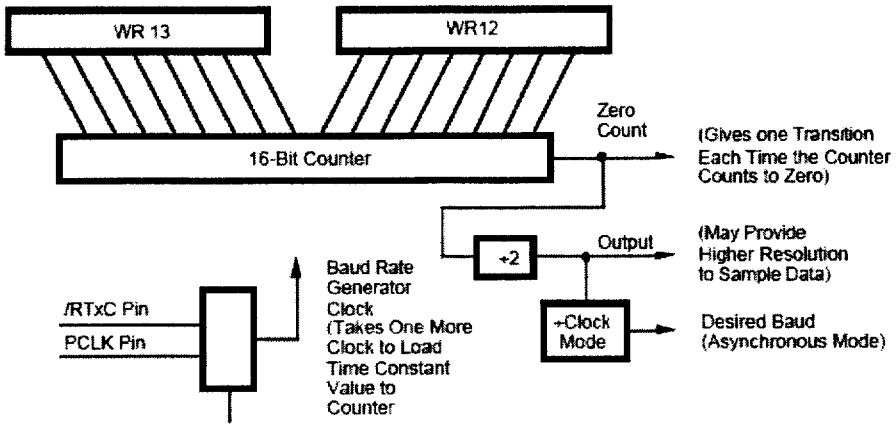


Figure 3-1. Baud Rate Generator

The formulas relating the baud rate to the time-constant and vice versa are shown below.

$$\text{Time Constant} = \frac{\text{Clock Frequency}}{2 \times (\text{Clock Mode}) \times (\text{Baud Rate})} - 2$$

$$\text{Baud Rate} = \frac{\text{Clock Frequency}}{2 \times (\text{Clock Mode}) \times (\text{Time Constant} + 2)}$$

5.1 INTRODUCTION

This section describes the functions of the various bits in the registers of the SCC (Tables 5-1 and 5-2). Reserved bits are not used in this implementation of the device and may or may not be physically present in the device. For the register addresses, also refer to Tables 2-1, 2-2 and 2-5 in Chapter 2. Reserved bits that are physically present are readable and writable but reserved bits that are not present will always be read as zero. To ensure compatibility with future versions of the device, reserved bits should always be written with zeros. Reserved commands are not used for the same reason.

Table 5-1. SCC Write Registers

Reg	Description
WR0	Reg. pointers, various initialization commands
WR1	Transmit and Receive interrupt enables, WAIT/DMA commands
WR2	Interrupt Vector
WR3[2]	Receive parameters and control modes
WR4[2]	Transmit and Receive modes and parameters
WR5[2]	Transmit parameters and control modes
WR6	Sync Character or SDLC address
WR7	Sync Character or SDLC flag
WR7'[1]	Extended Feature and FIFO Control (WR7 Prime)
WR8	Transmit buffer
WR9	Master Interrupt control and reset commands
WR10[2]	Miscellaneous transmit and receive control bits
WR11	Clock mode controls for receive and transmit
WR12	Lower byte of baud rate generator
WR13	Upper byte of baud rate generator
WR14	Miscellaneous control bits
WR15	External status interrupt enable control

Table 5-2. SCC Read Registers

Reg	Description
RR0	Transmit and Receive buffer status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only). Unmodified interrupt vector (Channel A only)
RR3	Interrupt pending bits (Channel A only)
RR4[2]	Transmit and Receive modes and parameters (WR4)
RR5[2]	Transmit parameters and control modes (WR5)
RR6[3]	SDLC FIFO byte counter lower byte (only when enabled)
RR7[3]	SDLC FIFO byte count and status (only when enabled)
RR8	Receive buffer
RR9[2]	Receive parameters and control modes (WR3)
RR10	Miscellaneous status bits
RR11[2]	Miscellaneous transmit and receive control bits (WR10)
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR14[2]	Extended Feature and FIFO Control (WR7 Prime)
RR15	External Status interrupt information

Notes for Tables 5-1 and 5-2:

1. ESCC and 85C30 only.
2. On the ESCC and 85C30, these registers are readable as RR9, RR4, RR5, and RR11, respectively, when WR7' D6=1. Refer to the description of WR7 Prime for enabling the extended read capability.
3. This feature is not available on NMOS.

5.2.5 Write Register 4 (Transmit/Receive Miscellaneous Parameters and Modes)

WR4 contains the control bits for both the receiver and the transmitter. These bits should be set in the transmit and receiver initialization routine before issuing the contents of WR1, WR3, WR6, and WR7. Bit positions for WR4 are shown in Figure 5-6. On the ESCC and 85C30, with the Extended Read option enabled, this register is read as RR4.

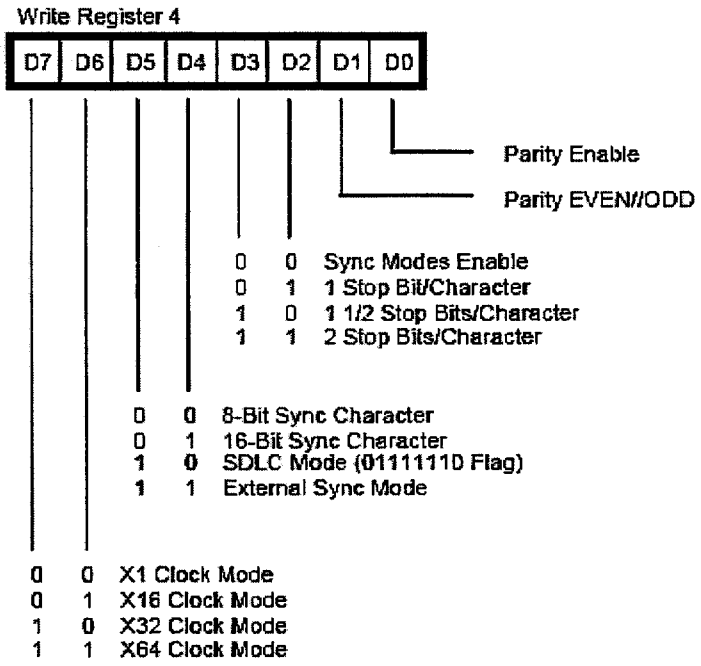


Figure 5-6. Write Register 4

5.2.6 Write Register 5 (Transmit Parameters and Controls)

WR5 contains control bits that affect the operation of the transmitter. D2 affects both the transmitter and the receiver. Bit positions for WR5 are shown in Figure 5-7. On the 85X30 with the Extended Read option enabled, this register is read as RR5.

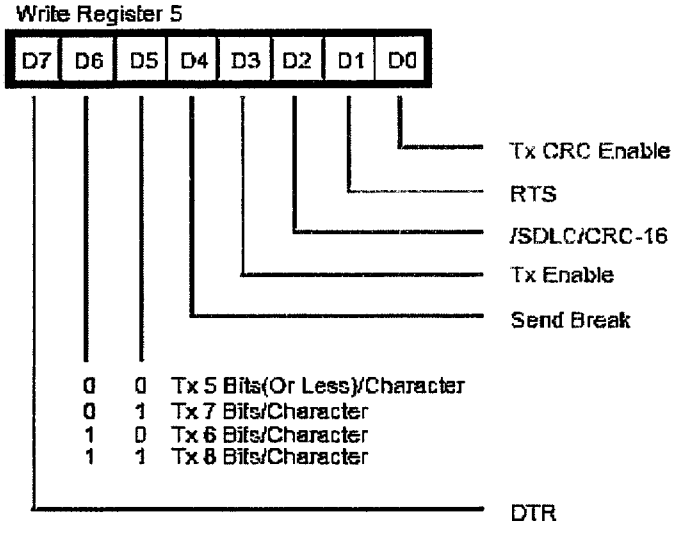


Figure 5-7. Write Register 5

5.2.15 Write Register 12 (Lower Byte of Baud Rate Generator Time Constant)

WR12 contains the lower byte of the time constant for the baud rate generator. The time constant can be changed at any time, but the new value does not take effect until the next time the time constant is loaded into the down counter. No attempt is made to synchronize the loading of the time constant into WR12 and WR13 with the clock driving the down counter. For this reason, it is advisable to disable the baud rate generator while the new time constant
is loaded into WR12 and WR13. Ordinarily, this is done anyway to prevent a load of the down counter between the writing of the upper and lower bytes of the time constant. The formula for determining the appropriate time constant for a given baud is shown below, with the desired rate in bits per second and the BR clock period in seconds. This formula is derived because the counter decrements from N down to zero-plus-one-cycle for reloading the time constant.
This is then fed to a toggle flip-flop to make the output a square wave. Bit positions for WR12 are shown in Figure 5-15.

$$\text{Time Constant} = \frac{\text{Clock Frequency}}{2 \times (\text{Desired Rate}) \times (\text{BR Clock Period})} - 2$$

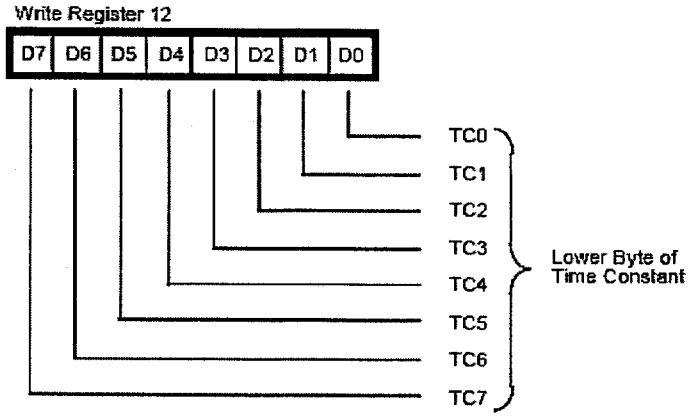


Figure 5-15. Write Register 12

5.2.16 Write Register 13 (Upper Byte of Baud Rate Generator Time Constant)

WR13 contains the upper byte of the time constant for the baud rate generator. Bit positions for WR13 are shown in Figure 5-16.

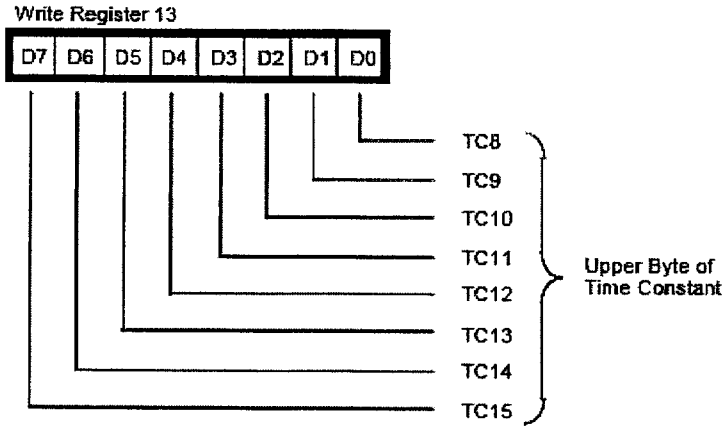


Figure 5-16. Write Register 13