B.E.P. MÉTIERS DE L'ÉLECTRONIQUE
Session 2006

DOCUMENTS
DES
CONSTRUCTEURS
DE COMPOSANTS ÉLECTRONIQUES

NÉCESSAIRES A L'ÉPREUVE EP3

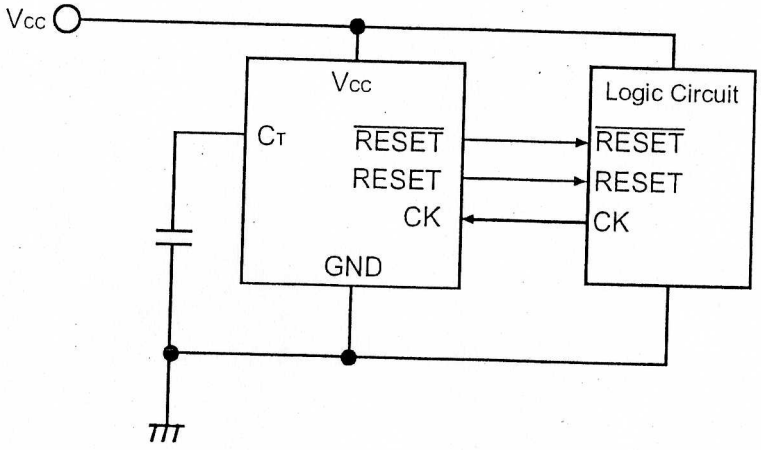
ANALYSE DES STRUCTURES ÉLECTRONIQUES APPARTENANT À UN OBJET TECHNIQUE

MB3773	**(pages 5 et 6 du document)**
Am27C512	**(page 1 du document)**
74HC139	**(page 4 du document)**
74HC541	**(page 3 et 4 du document)**
74HC574	**(page 4 du document)**
Pal22V10	**(page 8 du document)**
ULN2803	**(pages 1 et 2 du document)**
2N3055	**(page 1 du document)**

Soit 12 pages dont celle-ci.

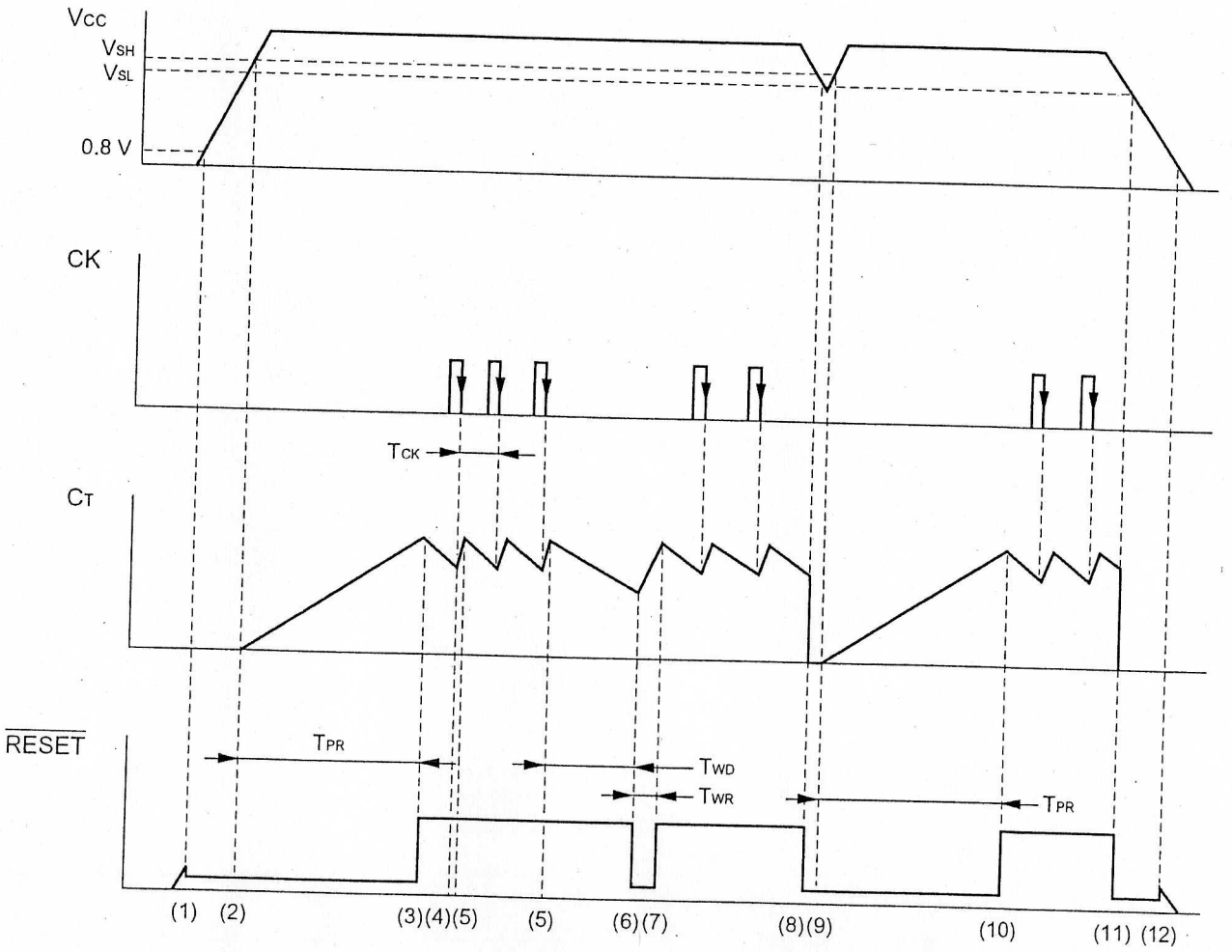
MB3773

• MB3773 Basic Operation



T_{PR} (ms) : = 1000 · C_T (µF)
T_{WD} (ms) := 100 · C_T (µF)
T_{WR} (ms) := 20 · C_T (µF)

Example : C_T = 0.1 µF
T_{PR} (ms) : = 100 (ms)
T_{WD} (ms) : = 10 (ms)
T_{WR} (ms) : = 2 (ms)



5

MB3773

■ OPERATION SEQUENCE

(1) When Vcc rises to about 0.8 V, $\overline{\text{RESET}}$ goes "Low" and RESET goes "High".
The pull-up current of approximately 1 μA (Vcc = 0.8 V) is output from RESET.

(2) When Vcc rises to V_{SH} (≒ 4.3V) , the charge with C_T starts.
At this time, the output is being reset.

(3) When C_T begins charging, $\overline{\text{RESET}}$ goes "High" and RESET goes "Low".
After T_{PR} reset of the output is released.
Reset hold time: T_{PR} (ms) ≒ 1000 × C_T (μF)
After releasing reset, the discharge of C_T starts, and watch-dog timer operation starts.
T_{PR} is not influenced by the CK input.

(4) C changes from the discharge into the charge if the clock (Negative edge) is input to the CK terminal while discharging C_T.

(5) C changes from the charge into the discharge when the voltage of C_T reaches a constant threshold (≒ 1.4 V) .
(4) and (5) are repeated while a normal clock is input by the logic system.

(6) When the clock is cut off, gets, and the voltage of C_T falls on threshold (≒ 0.4 V) of reset on, $\overline{\text{RESET}}$ goes "Low" and RESET goes "High".
Discharge time of C_T until reset is output: T_{WD} is watch-dog timer monitoring time.
T_{WD} (ms) ≒ 100 × C_T (μF)
Because the charging time of C_T is added at accurate time from stop of the clock and getting to the output of reset of the clock, T_{WD} becomes maximum T_{WD} + T_{WR} by minimum T_{WD}.

(7) Reset time in operating watch-dog timer:T_{WR} is charging time where the voltage of C_T goes up to off threshold (≒ 1.4 V) for reset.
T_{WR} (ms) ≒ 20 × C_T (μF)
Reset of the output is released after C_T reaches an off threshold for reset, and C_T starts the discharge, after that if the clock is normally input, operation repeats (4) and (5) , when the clock is cut off, operation repeats (6) and (7) .

(8) When Vcc falls on V_{SL} (≒ 4.2 V) , reset is output. C_T is rapidly discharged of at the same time.

(9) When Vcc goes up to V_{SH}, the charge with C_T is started.
When Vcc is momentarily low,
After falling V_{SL} or less Vcc, the time to going up is the standard value of the Vcc input pulse width in V_{SH} or more.
After the charge of C_T is discharged, the charge is started if it is T_{PI} or more.

(10) Reset of the output is released after T_{PR}, after Vcc becomes V_{SH} or more, and the watch-dog timer starts.
After that, when Vcc becomes V_{SL} or less, (8) to (10) is repeated.

(11) While power supply is off, when Vcc becomes V_{SL} or less, reset is output.

(12) The reset output is maintained until Vcc becomes 0.8 V when Vcc falls on 0 V.

FINAL

Am27C512

512 Kilobit (64 K x 8-Bit) CMOS EPROM

AMD

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - — Speed options as fast as 55 ns
- **Low power consumption**
  - — 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
- **Single +5 V power supply**
- **±10% power supply tolerance standard**
- **100% Flashrite™ programming**
  - — Typical programming time of 8 seconds
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions
- **Standard 28-pin DIP, PDIP, and 32-pin PLCC packages**

GENERAL DESCRIPTION

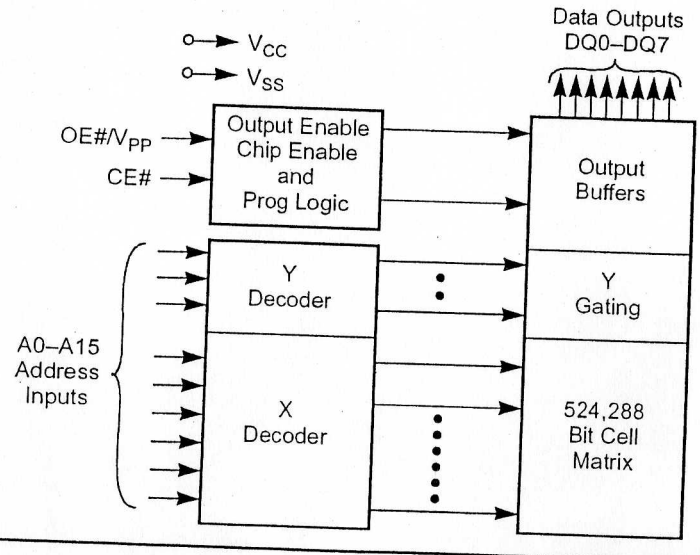
The Am27C512 is a 512-Kbit, ultraviolet erasable programmable read-only memory. It is organized as 64K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP packages, as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Data can be typically accessed in less than 55 ns, allowing high-performance microprocessors to operate without any WAIT states. The device offers separate Output Enable (OE#) and Chip Enable (CE#) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The device supports AMD's Flashrite programming algorithm (100 µs pulses), resulting in a typical programming time of 8 seconds.

BLOCK DIAGRAM



08140J-1

Publication# 08140 Rev: J Amendment/+2
Issue Date: June 1, 1999

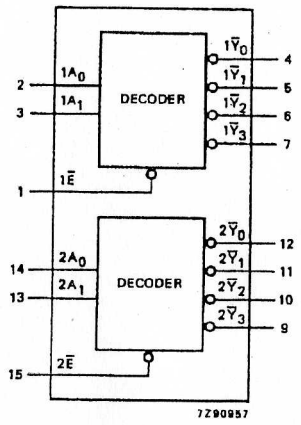


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\bar{E}$	nA_0	nA_1	$n\bar{Y}_0$	$n\bar{Y}_1$	$n\bar{Y}_2$	$n\bar{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

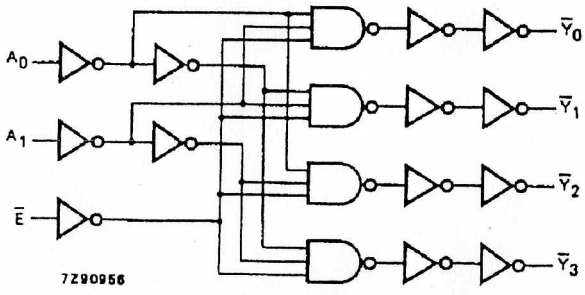


Fig.5 Logic diagram (one decoder/demultiplexer).

Octal buffer/line driver; 3-state 74HC/HCT541

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_7	bus outputs
20	V_{CC}	positive supply voltage

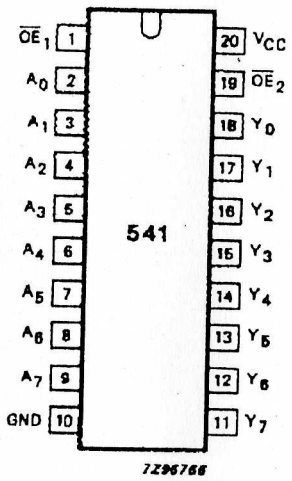


Fig.1 Pin configuration.

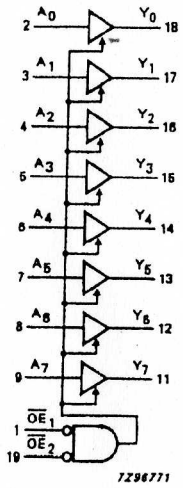


Fig.2 Logic symbol.

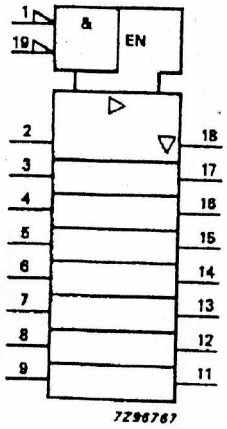


Fig.3 IEC logic symbol.

Octal buffer/line driver; 3-state

74HC/HCT541

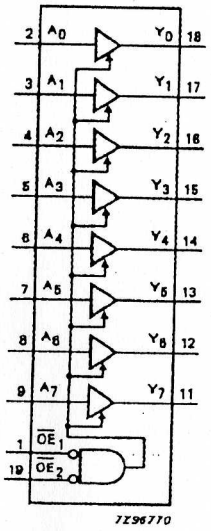


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   Z = high impedance OFF-state

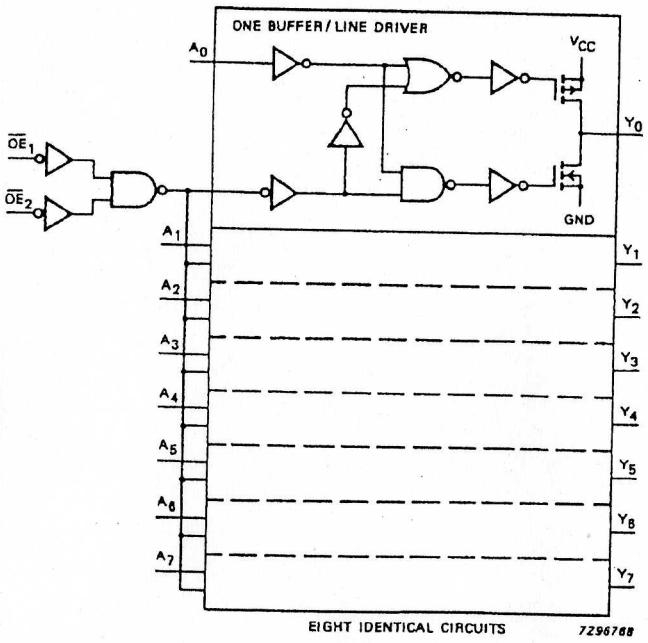


Fig.5 Logic diagram.

Octal D-type flip-flop; positive edge-trigger; 3-state

74HC/HCT574

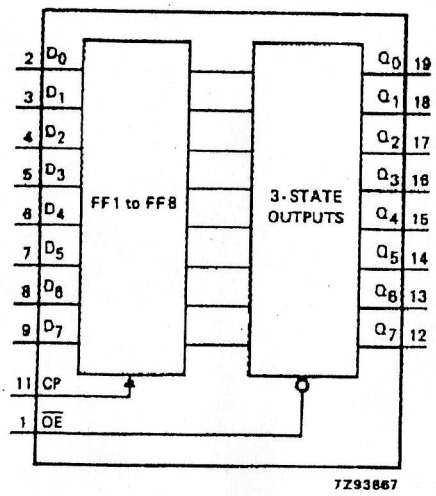


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level on set-up time prior to the LOW-to-HIGH CP transition
   Z = HIGH impedance OFF-state
   ↑ = LOW-to-HIGH clock transition

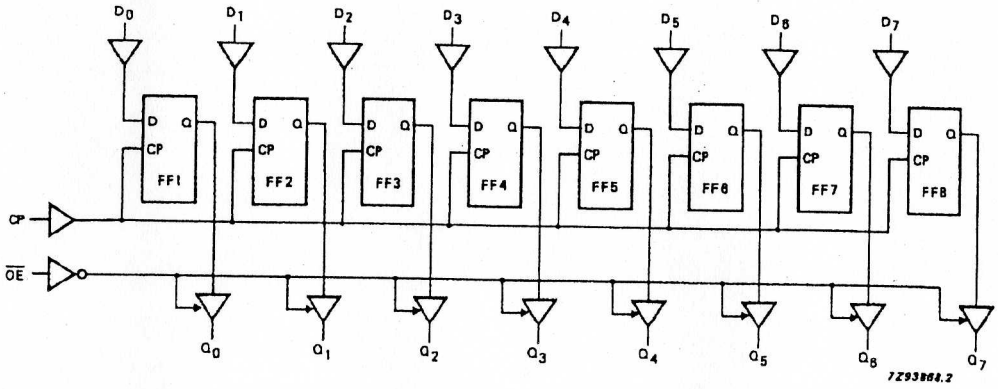


Fig.5 Logic diagram.

Lattice Semiconductor Corporation

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature with Power Applied . . . . . -55°C to +125°C

Supply Voltage with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to +5.25 V

DC Output or I/O Pin Voltage . . . . . -0.5 V to +5.25 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . -40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min	I_{OH} = -2 mA	2.4		V
			I_{OH} = -100 µA	V_{CC} -0.2		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 16 mA		0.5	V
			I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0	5.25	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			-100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			-100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		-5	-75	mA
I_{CC} (Static)	Supply Current	Outputs f = 0 MHz, Open (I_{OUT} = 0 mA)	-10/15 Commercial		60	mA
			-7		75	mA
			-15 Industrial		75	mA

Notes:

1. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

MOTOROLA

Order this document by ULN2803/D

Octal High Voltage, High Current Darlington Transistor Arrays

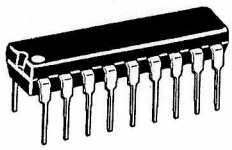
ULN2803
ULN2804

OCTAL PERIPHERAL DRIVER ARRAYS

SEMICONDUCTOR TECHNICAL DATA

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open–collector outputs and free wheeling clamp diodes for transient suppression.

The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.



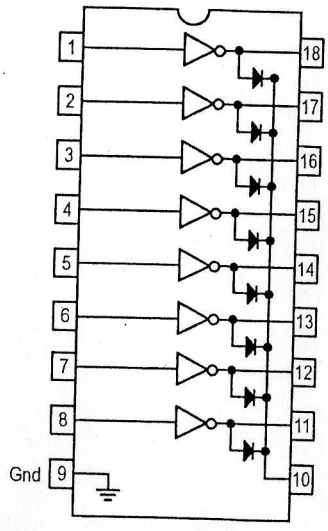
A SUFFIX
PLASTIC PACKAGE
CASE 707

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package, unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except ULN2801)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Junction Temperature	T_J	125	°C

$R_{\theta JA}$ = 55°C/W
Do not exceed maximum current limit per driver.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Characteristics		
	Input Compatibility	V_{CE}(Max)/I_C(Max)	Operating Temperature Range
ULN2803A ULN2804A	TTL, 5.0 V CMOS 6 to 15 V CMOS, PMOS	50 V/500 mA	T_A = 0 to + 70°C

Rev 1

ULN2803 ULN2804

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current (Figure 1)		I_{CEX}				µA
(V_O = 50 V, T_A = +70°C)	All Types		–	–	100	
(V_O = 50 V, T_A = +25°C)	All Types		–	–	50	
(V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	ULN2802		–	–	500	
(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	ULN2804		–	–	500	
Collector–Emitter Saturation Voltage (Figure 2)		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 µA)	All Types		–	1.1	1.6	
(I_C = 200 mA, I_B = 350 µA)	All Types		–	0.95	1.3	
(I_C = 100 mA, I_B = 250 µA)	All Types		–	0.85	1.1	
Input Current – On Condition (Figure 4)		$I_{I(on)}$				mA
(V_I = 17 V)	ULN2802		–	0.82	1.25	
(V_I = 3.85 V)	ULN2803		–	0.93	1.35	
(V_I = 5.0 V)	ULN2804		–	0.35	0.5	
(V_I = 12 V)	ULN2804		–	1.0	1.45	
Input Voltage – On Condition (Figure 5)		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2802		–	–	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2803		–	–	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	ULN2803		–	–	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2803		–	–	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	ULN2804		–	–	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2804		–	–	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	ULN2804		–	–	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	ULN2804		–	–	8.0	
Input Current – Off Condition (Figure 3) (I_C = 500 µA, T_A = +70°C)	All Types	$I_{I(off)}$	50	100	–	µA
DC Current Gain (Figure 2) (V_{CE} = 2.0 V, I_C = 350 mA)	ULN2801	h_{FE}	1000	–	–	–
Input Capacitance		C_I	–	15	25	pF
Turn–On Delay Time (50% E_I to 50% E_O)		t_{on}	–	0.25	1.0	µs
Turn–Off Delay Time (50% E_I to 50% E_O)		t_{off}	–	0.25	1.0	µs
Clamp Diode Leakage Current (Figure 6) (V_R = 50 V)	T_A = +25°C T_A = +70°C	I_R	–	–	50 100	µA
Clamp Diode Forward Voltage (Figure 7) (I_F = 350 mA)		V_F	–	1.5	2.0	V

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document by 2N3055/D

Complementary Silicon Power Transistors

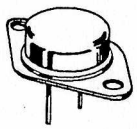
NPN 2N3055*
PNP MJ2955*

*Motorola Preferred Device

. . . designed for general–purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20–70 @ I_C = 4 Adc
- Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

15 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 60 VOLTS 115 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Emitter Voltage	V_{CER}	70	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

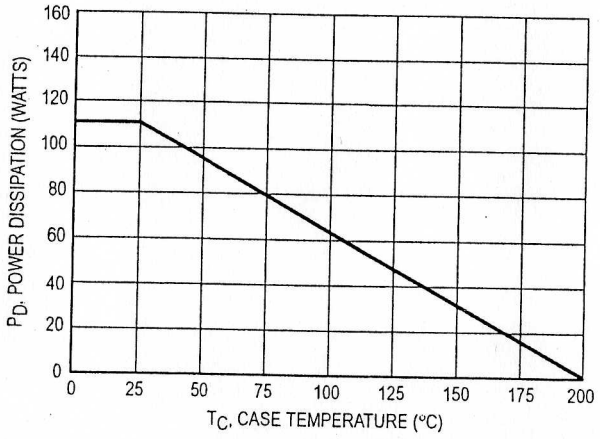


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

MOTOROLA