- *I2C*

OpenI2C
OpenI2C1
OpenI2C2

Function: Configure the SSPx module.

Include: `i2c.h`

Prototype:
```
void OpenI2C( unsigned char sync_mode,
              unsigned char slew );
void OpenI2C1( unsigned char sync_mode,
              unsigned char slew );
void OpenI2C2( unsigned char sync_mode,
              unsigned char slew );
```

Arguments:

sync_mode
One of the following values, defined in `i2c.h`

`SLAVE_7`	I^2C Slave mode, 7-bit address
`SLAVE_10`	I^2C Slave mode, 10-bit address
`MASTER`	I^2C Master mode

slew
One of the following values, defined in `i2c.h`

`SLEW_OFF`	Slew rate disabled for 100 kHz mode
`SLEW_ON`	Slew rate enabled for 400 kHz mode

Remarks: `OpenI2Cx` resets the SSPx module to the POR state and then configures the module for Master/Slave mode and the selected slew rate.

File Name:
`i2c_open.c`
`i2c1open.c`
`i2c2open.c`

Code Example:
```
OpenI2C(MASTER, SLEW_ON);
```

EEByteWrite

Function : Write a single byte to the I2C bus

Include : i2c.h

Prototype :
```
unsigned char EEByteWrite(
        Unsigned char control,
        Unsigned char addressH,
        Unsigned char addressL,
        Unsigned char data ) ;
```

Arguments

control : EEPROM control/ bus device select address byte.
addressH & addressL: EEPROM internal address location.
data : Data to write to EEPROM address specified in function parameter address

National Semiconductor

December 1999

LM2594/LM2594HV
SIMPLE SWITCHER® Power Converter 150 kHz 0.5A Step-Down Voltage Regulator

General Description

The LM2594/LM2594HV series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 0.5A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, and an adjustable output version, and are packaged in a 8-lead DIP and a 8-lead surface mount package.

Requiring a minimum number of external components, these regulators are simple to use and feature internal frequency compensation†, a fixed-frequency oscillator, and improved line and load regulation specifications.

The LM2594/LM2594HV series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Because of its high efficiency, the copper traces on the printed circuit board are normally the only heat sinking needed.

A standard series of inductors (both through hole and surface mount types) are available from several different manufacturers optimized for use with the LM2594/LM2594HV series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 85 µA standby current. Self protection features include a two stage frequency reducing current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

The LM2594HV is for applications requiring an input voltage up to 60V.

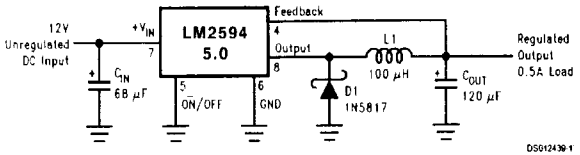
Features

- 3.3V, 5V, 12V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 37V (57V for the HV version)±4% max over line and load conditions
- Available in 8-pin surface mount and DIP-8 package
- Guaranteed 0.5A output current
- Input voltage range up to 60V
- Requires only 4 external components
- 150 kHz fixed frequency internal oscillator
- TTL Shutdown capability
- Low power standby mode, I_Q typically 85 µA
- High Efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative convertor

Typical Application (Fixed Output Voltage Versions)



SIMPLE SWITCHER and *Switchers Made Simple*™ are registered trademarks of National Semiconductor Corporation

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Maximum Supply Voltage	
LM2594	45V
LM2594HV	60V
$\overline{ON}$ /OFF Pin Input Voltage	−0.3 ≤ V ≤ +25V
Feedback Pin Voltage	−0.3 ≤ V ≤+25V
Output Voltage to Ground (Steady State)	−1V
Power Dissipation	Internally limited
Storage Temperature Range	−65˚C to +150˚C
ESD Susceptibility	
Human Body Model (Note 2)	2 kV
Lead Temperature	
M8 Package	
Vapor Phase (60 sec.)	+215˚C
Infrared (15 sec.)	+220˚C
N Package (Soldering, 10 sec.)	+260˚C
Maximum Junction Temperature	+150˚C

Operating Conditions

Temperature Range	−40˚C ≤ T_J +125˚C
Supply Voltage	
LM2594	4.5V to 40V
LM2594HV	4.5V to 60V

LM2594/LM2594HV-3.3 Electrical Characteristics

Specifications with standard type face are for T_J = 25˚C, and those with **boldface type** apply over **full Operating Temperature Range.** V_{INmax} = 40V for the LM2594 and 60V for the LM2594HV.

Symbol	Parameter	Conditions	LM2594/LM2594HV-3.3 Typ (Note 3)	LM2594/LM2594HV-3.3 Limit (Note 4)	Units (Limits)
SYSTEM PARAMETERS (Note 5) Test Circuit *Figure 1*					
V_{OUT}	Output Voltage	4.75V ≤ V_{IN} ≤ V_{INmax}, 0.1A ≤ I_{LOAD} ≤ 0.5A	3.3		V
				3.168/**3.135**	V(min)
				3.432/**3.465**	V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.5A	80		%

LM2594/LM2594HV-5.0 Electrical Characteristics

Specifications with standard type face are for T_J = 25˚C, and those with **boldface type** apply over **full Operating Temperature Range**

Symbol	Parameter	Conditions	LM2594/LM2594HV-5.0 Typ (Note 3)	LM2594/LM2594HV-5.0 Limit (Note 4)	Units (Limits)
SYSTEM PARAMETERS (Note 5) Test Circuit *Figure 1*					
V_{OUT}	Output Voltage	7V ≤ V_{IN} ≤ V_{INmax}, 0.1A ≤ I_{LOAD} ≤ 0.5A	5.0		V
				4.800/**4.750**	V(min)
				5.200/**5.250**	V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.5A	82		%

LM2594/LM2594HV-12 Electrical Characteristics

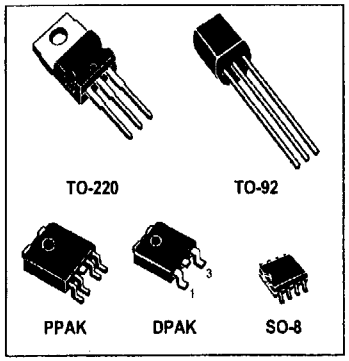
Specifications with standard type face are for T_J = 25˚C, and those with **boldface type** apply over **full Operating Temperature Range**

Symbol	Parameter	Conditions	LM2594/LM2594HV-12 Typ (Note 3)	LM2594/LM2594HV-12 Limit (Note 4)	Units (Limits)
SYSTEM PARAMETERS (Note 5) Test Circuit *Figure 1*					
V_{OUT}	Output Voltage	15V ≤ V_{IN} ≤ V_{INmax}, 0.1A ≤ I_{LOAD} ≤ 0.5A	12.0		V
				11.52/**11.40**	V(min)
				12.48/**12.60**	V(max)
η	Efficiency	V_{IN} = 25V, I_{LOAD} = 0.5A	88		%

L4931 SERIES

VERY LOW DROP VOLTAGE REGULATORS WITH INHIBIT

- VERY LOW DROPOUT VOLTAGE (0.4V)
- VERY LOW QUIESCENT CURRENT (TYP. 50 µA IN OFF MODE, 600µA IN ON MODE)
- OUTPUT CURRENT UP TO 250 mA
- LOGIC-CONTROLLED ELECTRONIC SHUTDOWN
- OUTPUT VOLTAGES OF 1.25; 1.5; 2.5; 2.7; 3; 3.3; 3.5; 4; 4.5; 4.7; 5; 5.2; 5.5; 6; 8; 12V
- INTERNAL CURRENT AND THERMAL LIMIT
- ONLY 2.2µF FOR STABILITY
- AVAILABLE IN ± 1% (AB) OR 2% (C) SELECTION AT 25 °C
- SUPPLY VOLTAGE REJECTION: 70db TYP. FOR 5V VERSION
- TEMPERATURE RANGE: -40 TO 125 °C



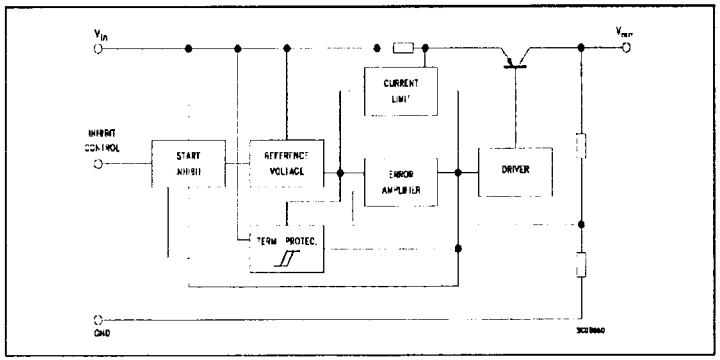
DESCRIPTION

The L4931 series are very Low Drop regulators available in TO-220, SO-8, DPAK, PPAK and TO-92 packages and in a wide range of output voltages.

The very Low Drop voltage (0.4V) and the very low quiescent current make them particularly suitable for Low Noise, Low Power applications and specially in battery powered systems.

In PPAK and SO-8 packages a Shutdown Logic Control function is available TTL compatible. This means that when the device is used as a local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. It requires only a 2.2 µF capacitor for stability allowing space and cost saving.

SCHEMATIC DIAGRAM

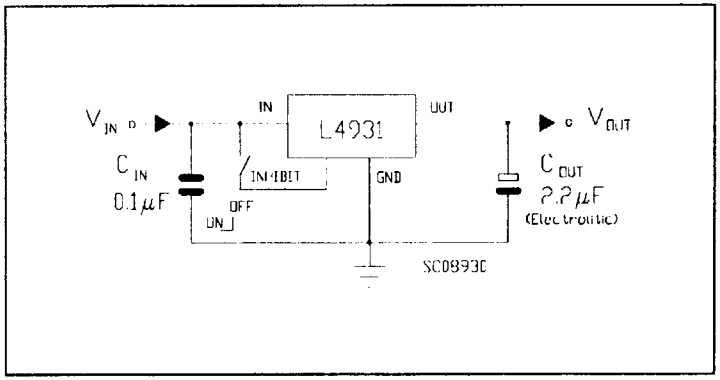


ORDERING NUMBERS

TO-220	SO-8	PPAK	DPAK	TO-92	Output Voltage
L4931CV12 (*)	L4931CD12 (*)	L4931CPT12 (*)	L4931CDT12 (*)	L4931CZ12 (*)	1.25 V
L4931ABV12 (*)	L4931ABD12 (*)	L4931ABPT12 (*)	L4931ABDT12 (*)	L4931ABZ12 (*)	1.25 V
L4931CV15 (*)	L4931CD15 (*)	L4931CPT15 (*)	L4931CDT15 (*)	L4931CZ15 (*)	1.5 V
L4931ABV15 (*)	L4931ABD15 (*)	L4931ABPT15 (*)	L4931ABDT15 (*)	L4931ABZ15 (*)	1.5 V
L4931CV25 (*)	L4931CD25 (*)	L4931CPT25 (*)	L4931CDT25 (*)	L4931CZ25 (*)	2.5 V
L4931ABV25 (*)	L4931ABD25 (*)	L4931ABPT25 (*)	L4931ABDT25 (*)	L4931ABZ25 (*)	2.5 V
L4931CV27	L4931CD27	L4931CPT27	L4931CDT27	L4931CZ27	2.7 V
L4931ABV27	L4931ABD27	L4931ABPT27	L4931ABDT27	L4931ABZ27	2.7 V
L4931CV30	L4931CD30	L4931CPT30	L4931CDT30	L4931CZ30	3 V
L4931ABV30	L4931ABD30	L4931ABPT30	L4931ABDT30	L4931ABZ30	3 V
L4931CV33	L4931CD33	L4931CPT33	L4931CDT33	L4931CZ33	3.3 V
L4931ABV33	L4931ABD33	L4931ABT33	L4931ABDT33	L4931ABZ33	3.3 V
L4931CV35	L4931CD35	L4931CPT35	L4931CDT35	L4931CZ35	3.5 V
L4931ABV35	L4931ABD35	L4931ABPT35	L4931ABDT35	L4931ABZ35	3.5 V
L4931CV40	L4931CD40	L4931CPT40	L4931CDT40	L4931CZ40	4 V
L4931ABV40	L4931ABD40	L4931ABPT40	L4931ABDT40	L4931ABZ40	4 V
L4931CV45 (*)	L4931CD45 (*)	L4931CPT45 (*)	L4931CDT45 (*)	L4931CZ45 (*)	4.5 V
L4931ABV45 (*)	L4931ABD45 (*)	L4931ABPT45 (*)	L4931ABDT45 (*)	L4931ABZ45 (*)	4.5 V
L4931CV47	L4931CD47	L4931CPT47	L4931CDT47	L4931CZ47	4.75 V
L4931ABV47	L4931ABD47	L4931ABPT47	L4931ABDT47	L4931ABZ47	4.75 V
L4931CV50	L4931CD50	L4931CPT50	L4931CDT50	L4931CZ50	5 V
L4931ABV50	L4931ABD50	L4931ABPT50	L4931ABDT50	L4931ABZ50	5 V
L4931CV52 (*)	L4931CD52 (*)	L4931CPT52 (*)	L4931CDT52 (*)	L4931CZ52 (*)	5.2 V
L4931ABV52 (*)	L4931ABD52 (*)	L4931ABPT52 (*)	L4931ABDT52 (*)	L4931ABZ52 (*)	5.2 V
L4931CV55 (*)	L4931CD55 (*)	L4931CPT55 (*)	L4931CDT55 (*)	L4931CZ55 (*)	5.5 V
L4931ABV55 (*)	L4931ABD55 (*)	L4931ABPT55 (*)	L4931ABDT55 (*)	L4931ABZ55 (*)	5.5 V
L4931CV60	L4931CD60	L4931CPT60	L4931CDT60	L4931CZ60	6 V
L4931ABV60	L4931ABD60	L4931ABPT60	L4931ABDT60	L4931ABZ60	6 V
L4931CV80	L4931CD80	L4931CPT80	L4931CDT80	L4931CZ80	8 V
L4931ABV80	L4931ABD80	L4931ABPT80	L4931ABDT80	L4931ABZ80	8 V
L4931CV120	L4931CD120	L4931CPT120	L4931CDT120	L4931CZ120	12 V
L4931ABV120	L4931ABD120	L4931ABPT120	L4931ABDT120	L4931ABZ120	12 V

(*) Available on request

TEST CIRCUITS



MICROCHIP MCP601/602/603/604

2.7V to 5.5V Single Supply CMOS Op Amps

FEATURES

- Specifications rated from 2.7V to 5.5V supplies
- Rail-to-rail swing at output
- Common-mode input swing below ground
- 2.8MHz GBWP
- Unity gain stable
- Low power I_{DD} = 325µA max
- Chip Select capability with MCP603
- Industrial temperature range (-40°C to 85°C)
- Available in single, dual and quad

APPLICATIONS

- Portable Equipment
- A/D Converter Driver
- Photodiode Pre-amps
- Analog Filters
- Data Acquisition
- Notebooks and PDAs
- Sensor Interface

AVAILABLE TOOLS

- Spice Macromodels (at www.microchip.com)
- **FilterLab™** Software (at www.microchip.com)

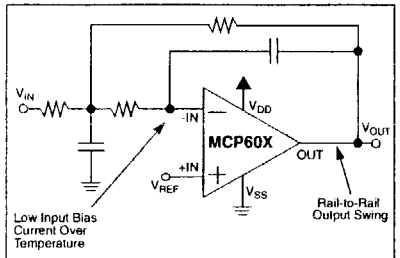
DESCRIPTION

The Microchip Technology Inc. MCP601/602/603/604 family of low power operational amplifiers are offered in single (MCP601), single with a Chip Select pin feature (MCP603), dual (MCP602) and quad (MCP604) configurations. These operational amplifiers (op amps) utilize an advanced CMOS technology, which provides low bias current, high speed operation, high open-loop gain and rail-to-rail output swing. This product offering operates with a single supply voltage that can be as low as 2.7V, while drawing less than 325µA of quiescent current. In addition, the common-mode input voltage range goes 0.3V below ground, making these amplifiers ideal for single supply operation.

These devices are appropriate for low-power battery operated circuits due to the low quiescent current, for A/D Converter driver amplifiers because of their wide bandwidth, or for anti-aliasing filters by virtue of their low input bias current.

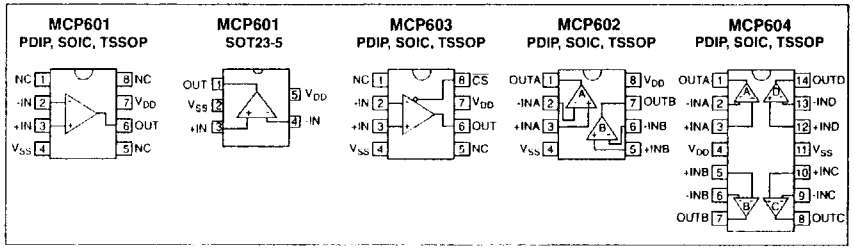
The MCP601, MCP602 and MCP603 are available in standard 8-lead PDIP, SOIC and TSSOP packages. The MCP601 is also available in the SOT23-5 package. The quad MCP604 is offered in 14-lead PDIP, SOIC and TSSOP packages. PDIP and SOIC packages are fully specified from -40°C to +85°C with power supplies from 2.7V to 5.5V.

TYPICAL APPLICATION



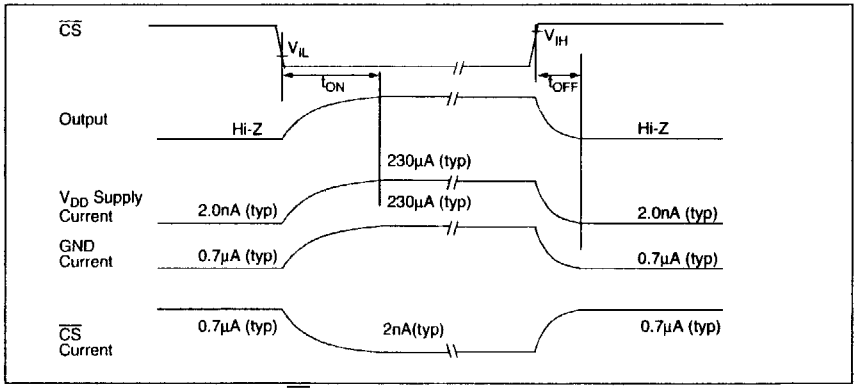
2nd Order Low Pass Filter

PACKAGES



3.4 The Chip Select Option of the MCP603

The MCP603 is a single amplifier with a Chip Select option. When $\overline{CS}$ is pulled high the supply current drops to 0.7µA (typ), which is pulled through the $\overline{CS}$ pin to V_{SS}. In this state, the amplifier is put into a high impedance state. By pulling $\overline{CS}$ low or letting the pin float, the amplifier is enabled. Figure 3-6 shows the output voltage and supply current response to a $\overline{CS}$ pulse.



MCP60X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

MCP60X — X /X

Package:
- P = Plastic DIP (300 mil Body), 8-lead and 14-lead
- SN = Plastic SOIC (150 mil Body), 8-lead
- SL = Plastic SOIC (150 mil Body), 14-lead
- ST = Plastic TSSOP, 8-lead and 14-lead
- OT = Plastic SOT23, 5-lead

Temperature Range:
- I = -40°C to +85°C

Device:
- MCP601 = Single Operational Amplifier
- MCP601T = Single Operational Amplifier (Tape and Reel-SOIC/TSSOP/SOT23-5)
- MCP602 = Dual Operational Amplifier
- MCP602T = Dual Operational Amplifier (Tape and Reel-SOIC/TSSOP)
- MCP603 = Single Operational Amplifier w/$\overline{CS}$ Function
- MCP603T = Single Operational Amplifier w/$\overline{CS}$ Function (Tape and Reel-SOIC/TSSOP)
- MCP604 = Quad Operational Amplifier
- MCP604T = Quad Operational Amplifier (Tape and Reel-SOIC/TSSOP)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 786-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

FM24CL64

64Kb Serial 3V FRAM Memory

Features

64K bit Ferroelectric Nonvolatile RAM
- Organized as 8,192 x 8 bits
- Unlimited Read/Write Cycles
- 10 year Data Retention
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Fast Two-wire Serial Interface
- Up to 1 MHz maximum bus frequency
- Direct hardware replacement for EEPROM
- Supports legacy timing for 100 kHz & 400 kHz

Low Power Operation
- True 2.7V-3.6V Operation
- 75 µA Active Current (100 kHz)
- 1 µA Standby Current

Industry Standard Configuration
- Industrial Temperature -40° C to +85° C
- 8-pin SOIC

Description

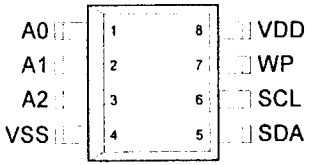
The FM24CL64 is a 64-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile and performs reads and writes like a RAM. It provides reliable data retention for 10 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

The FM24CL64 performs write operations at bus speed. No write delays are incurred. The next bus cycle may commence immediately without the need for data polling. In addition, the product offers write endurance orders of magnitude higher than EEPROM. Also, FRAM exhibits much lower power during writes than EEPROM since write operations do not require an internally elevated power supply voltage for write circuits.

These capabilities make the FM24CL64 ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows more frequent data writing with less overhead for the system.

The FM24CL64 provides substantial benefits to users of serial EEPROM, yet these benefits are available in a hardware drop-in replacement. The FM24CL64 is provided in industry standard 8-pin surface mount package using a familiar two-wire protocol. It is guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Pin Names	Function
A0-A2	Device Select Address
SDA	Serial Data/address
SCL	Serial Clock
WP	Write Protect
VSS	Ground
VDD	Supply Voltage

Ordering Information	
FM24CL64-S	8-pin SOIC

Ramtron International Corporation
1850 Ramtron Drive, Colorado Springs, CO 80921
(800) 545-FRAM, (719) 481-7000, Fax (719) 481-7058
www.ramtron.com

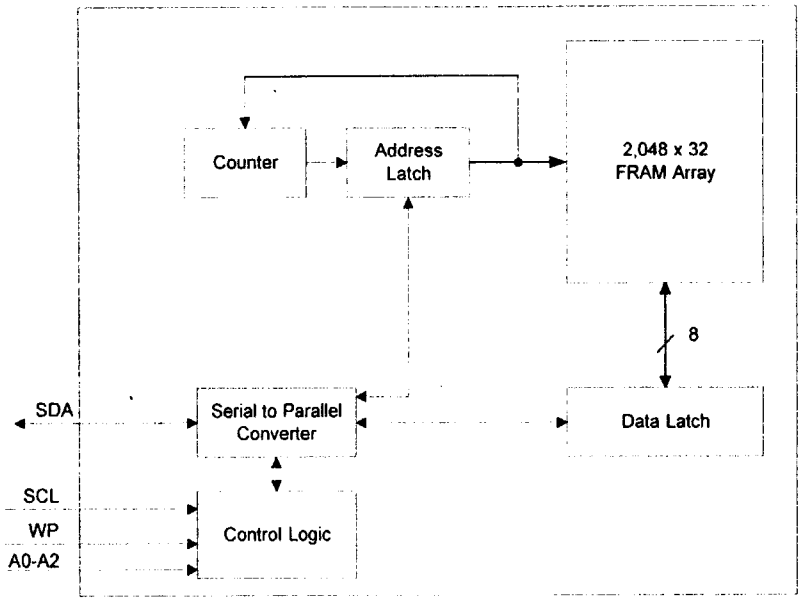


Figure 1. FM24CL64 Block Diagram

Pin Description

Pin Name	Type	Pin Description
A0-A2	Input	Address 0-2. These pins are used to select one of up to 8 devices of the same type on the same two-wire bus. To select the device, the address value on the three pins must match the corresponding bits contained in the device address. The address pins are pulled down internally.
SDA	I/O	Serial Data Address. This is a bi-directional line for the two-wire interface. It is open-drain and is intended to be wire-OR'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. A pull-up resistor is required.
SCL	Input	Serial Clock. The serial clock line for the two-wire interface. Data is clocked out of the part on the falling edge, and in on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
WP	Input	Write Protect. When tied to VDD, addresses in the entire memory map will be write-protected. When WP is connected to ground, all addresses may be written. This pin is pulled down internally.
VDD	Supply	Supply Voltage: 2.7V to 3.6V
VSS	Supply	Ground

Slave ID				Device Select			
1	0	1	0	A2	A1	A0	R/W
7	6	5	4	3	2	1	0

Figure 4. Slave Address

Addressing Overview

After the FM24CL64 (as receiver) acknowledges the device address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The first is the MSB. Since the device uses only 13 address bits, the value of the upper three bits are don't care. Following the MSB is the LSB with the remaining eight address bits. The address value is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch -- either a newly written value or the address following the last access. The current address will be held for as long as power remains or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24CL64 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (1FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Data Transfer

After the address information has been transmitted, data transfer between the bus master and the FM24CL64 can begin. For a read operation the FM24CL64 will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM24CL64 will transfer the next sequential byte. If the acknowledge is not sent, the FM24CL64 will end the read operation. For a write operation, the FM24CL64 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24CL64 is designed to operate in a manner very similar to other 2-wire interface memory products. The major differences result from the higher performance write capability of FRAM technology. These improvements result in some differences between the FM24CL64 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

Write Operation

All writes begin with a device address, then a memory address. The bus master indicates a write operation by setting the LSB of the device address to a 0. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 1FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using start or stop condition prior to the 8th data bit. The FM24CL64 uses no page buffering.

The memory array can be write protected using the WP pin. Setting the WP pin to a high condition (VDD) will write-protect all addresses. The FM24CL64 will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a low state (VSS) will deactivate this feature. WP is pulled down internally.

Figure 5 below illustrates both a single-byte and multiple-write.

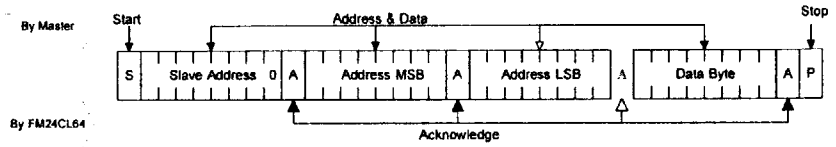


Figure 5. Single Byte Write

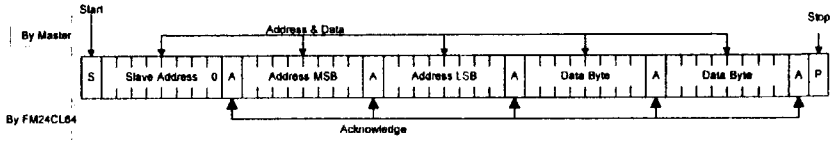


Figure 6. Multiple Byte Write

Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM24CL64 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM24CL64 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a device address with the LSB set to 1. This indicates that a read operation is requested. After receiving the complete device address, the FM24CL64 will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Each time the bus master acknowledges a byte, this indicates that the FM24CL64 should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24CL64 attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a stop in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a start in the 10th.
3. The bus master issues a stop in the 9th clock cycle.
4. The bus master issues a start in the 9th clock cycle.

If the internal address reaches 1FFFh, it will wrap around to 0000h on the next read cycle. Figures 7 and 8 below show the proper operation for current address reads.

Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

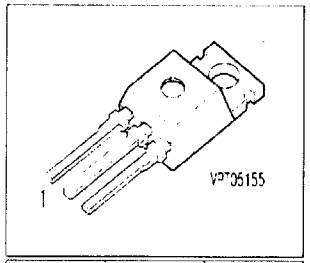
To perform a selective read, the bus master sends out the device address with the LSB set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes

SIEMENS

BUZ 60

SIPMOS ® Power Transistor

- N channel
- Enhancement mode
- Avalanche-rated



Pin 1	Pin 2	Pin 3
G	D	S

Type	V_{DS}	I_D	$R_{DS(on)}$	Package	Ordering Code
BUZ 60	400 V	5.5 A	1 Ω	TO-220 AB	C67078-S1312-A2

Maximum Ratings

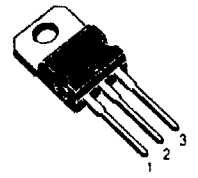
Parameter	Symbol	Values	Unit
Continuous drain current T_C = 36 °C	I_D	5.5	A
Pulsed drain current T_C = 25 °C	I_{Dpuls}	22	
Avalanche current,limited by T_{jmax}	I_{AR}	5.5	
Avalanche energy,periodic limited by T_{jmax}	E_{AR}	8	mJ
Avalanche energy, single pulse I_D = 5.5 A, V_{DD} = 50 V, R_{GS} = 25 Ω L = 18.5 mH, T_j = 25 °C	E_{AS}	320	
Gate source voltage	V_{GS}	± 20	V
Power dissipation T_C = 25 °C	P_{tot}	75	W
Operating temperature	T_j	-55 ... + 150	°C
Storage temperature	T_{stg}	-55 ... + 150	
Thermal resistance, chip case	R_{thJC}	≤ 1.67	K/W
Thermal resistance, chip to ambient	R_{thJA}	75	
DIN humidity category, DIN 40 040		E	
IEC climatic category, DIN IEC 68-1		55 / 150 / 56	

BUZ11

N - CHANNEL 50V - 0.03Ω - 33A TO-220
STripFET™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ11	50 V	< 0.04 Ω	33 A

- TYPICAL $R_{DS(on)}$ = 0.03 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE

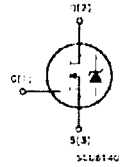


TO-220

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	50	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	50	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	33	A
I_{DM}	Drain Current (pulsed)	134	A
P_{tot}	Total Dissipation at T_c = 25 °C	90	W
T_{stg}	Storage Temperature	-65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 19 A		0.03	0.04	Ω

$R_{thj-case}$	Thermal Resistance Junction-case	Max	1.67	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W

BUZ60 - BUZ11

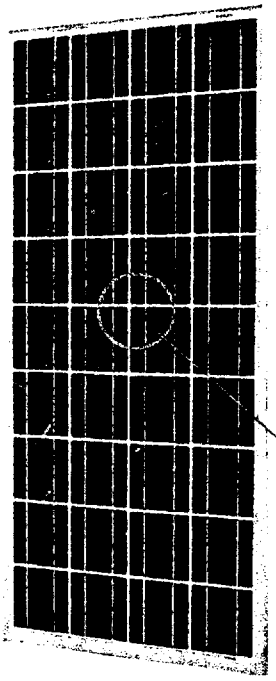
PANNEAU SOLAIRE

PHOTOWATT INTERNATIONAL S.A.

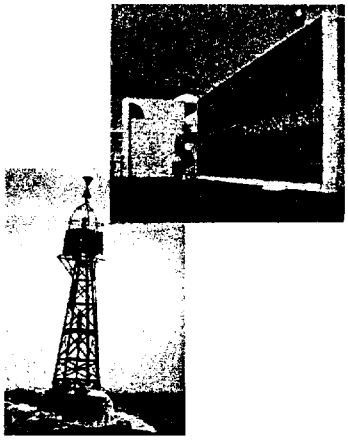
Solutions for natural power

SURTEC INGENIERIE

PWX500- 12 V
HAUTE FIABILITE
MODULE PHOTOVOLTAIQUE - JBox



- Télécommunication
- Télévision communautaire
- Protection cathodique
- Signalisation
- Hôpital, dispensaire de brousse
- Electrification rurale
- Pompage
- Couplage au réseau



Le PWX500 est fabriqué à partir de 4 X 9 cellules polycristallines 4 pouces (101,50 mm X 101,50 mm) à haut rendement.

Le PWX500 est un module bi-verre, parfaitement adapté aux conditions climatiques et environnementales sévères grâce au verre en face avant et en face arrière qui lui confère un isolement électrique et une fiabilité accrus.

Le module PWX500 utilise la technologie des cellules multicristallines PHOTOWATT. Les cellules solaires sont mesurées individuellement et triées électroniquement avant d'être interconnectées. L'encapsulation des cellules est réalisée entre deux plaques de verre trempé. L'encapsulant, de l'EVA résistant aux UV, enrobe les cellules photovoltaïques à l'intérieur des laminés protégeant ainsi les cellules de la corrosion. Le PWX500 bénéficie donc des garanties de l'excellente résistance mécanique du verre, à la fois en face avant et en face arrière.

Le cadre auto-porteur en aluminium anodisé a été étudié pour permettre une facilité de fixation tant par l'avant que par l'arrière. Ce module est disponible en version verre / tedlar PW500, plus léger tout en bénéficiant de propriétés électriques identiques .

Pour les applications intégrées au bâtiment sur structure existante, ce module peut être livré sans le cadre aluminium. Veuillez nous consulter pour tout complément d'information.

GARANTIE PUISSANCE : 25 ANS*

GARANTIE PRODUIT : 5 ANS*

PWX500		Configuration 12 V		
Puissance typique	**W**	45	50	55
Puissance minimale	**W**	40,1	45,1	50,1
Tension à la puissance typique	**V**	16,9	17,2	17,3
Intensité à la puissance typique	**A**	2,65	2,9	3,2
Intensité de court circuit	**A**	2,95	3,1	3,45
Tension en circuit ouvert	**V**	21,6	21,6	21,7
Tension maximum du circuit	**V**	**600V DC**		
Coefficients de température		α = +0,95 mA/°C ; β = -79 mV/°C ; γ P/P = - 0,43 % /°C		
Spécifications de puissance à 1000 W/m² : 25°C : AM 1,5				

*Selon les conditions générales de garantie

Informations sujettes à évolutions - Dernière mise à jour : Septembre 2003

PRECISION 2.5 VOLT LOW KNEE CURRENT VOLTAGE REFERENCE

ZRC250

ISSUE 3 - MARCH 1998

DEVICE DESCRIPTION

The ZRC250 uses a bandgap circuit design to achieve a precision micropower voltage reference of 2.5 volts. The device is available in small outline surface mount packages, ideal for applications where space saving is important, as well as packages for through hole requirements.

The ZRC250 design provides a stable voltage without an external capacitor and is stable with capacitive loads. The ZRC250 is recommended for operation between 20µA and 5mA and so is ideally suited to low power and battery powered applications.

Excellent performance is maintained to an absolute maximum of 25mA, however the rugged design and 20 volt processing allows the reference to withstand transient effects and currents up to 200mA. Superior switching capability allows the device to reach stable operating conditions in only a few microseconds.

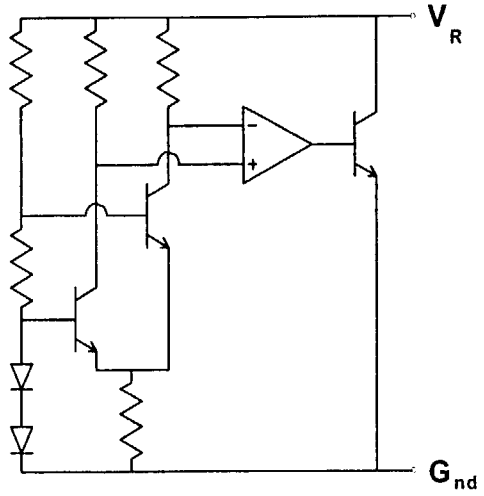
FEATURES

- Small outline SOT23 and SO8 packages
- TO92 style packages
- No stabilising capacitor required
- Low knee current, 15µA typical
- Typical T_C 30ppm/°C
- Typical slope resistance 0.4Ω
- ± 3, 2 and 1% tolerance
- Industrial temperature range
- Operating current 20µA to 5mA
- Transient response, stable in less than 10µs
- Optional extended current range

APPLICATIONS

- Battery powered and portable equipment.
- Instrumentation.
- Test equipment.

SCHEMATIC DIAGRAM



ZRC250

ABSOLUTE MAXIMUM RATING

Reverse Current	25mA
Forward Current	25mA
Operating Temperature	-40 to 85°C
Storage Temperature	-55 to 125°C

Power Dissipation (T_{amb}=25°C)

SOT23	330mW
E-line, 3 pin (TO92)	500mW
E-line, 2 pin (TO92)	500mW
SO8	625mW

ELECTRICAL CHARACTERISTICS

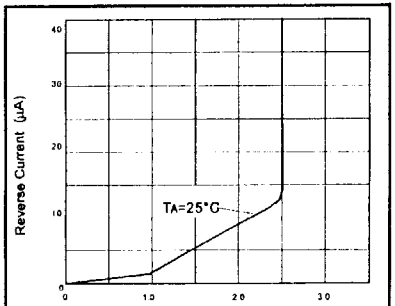
TEST CONDITIONS (Unless otherwise stated) T_{amb}=25°C

SYMBOL	PARAMETER	CONDITIONS	LIMITS			TOL%	UNITS
			MIN	TYP	MAX		
V_R	Reverse Breakdown Voltage	I_R=150µA	2.475 2.45 2.425	2.5 2.5 2.5	2.525 2.55 2.575	1 2 3	V
I_{MIN}	Minimum Operating Current			13	20		µA
I_R	Recommended Operating Current		0.02		5		mA
T_C †	Average Reverse Breakdown Voltage Temp. Co.	$I_{R(min)}$ to $I_{R(max)}$		30	90		ppm/°C
R_S §	Slope Resistance			0.4	1		Ω
Z_R	Reverse Dynamic Impedance	I_R = 1mA f = 100Hz I_{AC}=0.1 I_R		0.3	0.8		Ω
E_N	Wideband Noise Voltage	I_R= 150µA f = 10Hz to 10kHz		60			µV(rms)

† $$T_C = \frac{(V_{R(max)} - V_{R(min)}) \times 1000000}{V_R \times (T_{(max)} - T_{(min)})}$$

Note: $V_{R(max)}$ - $V_{R(min)}$ is the maximum deviation in reference voltage measured over the full operating temperature range.

§ $$R_S = \frac{V_R \text{ Change}(I_{R(min)} \text{ to } I_{R(max)})}{I_{R(max)} - I_{R(min)}}$$



Reverse Characteristics