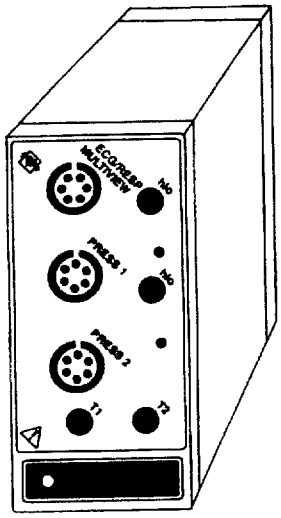
DOCUMENTATION

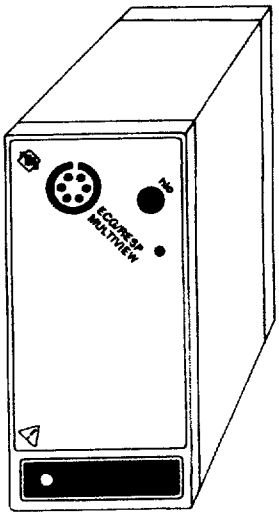
SOMMAIRE

DOCUMENTATION

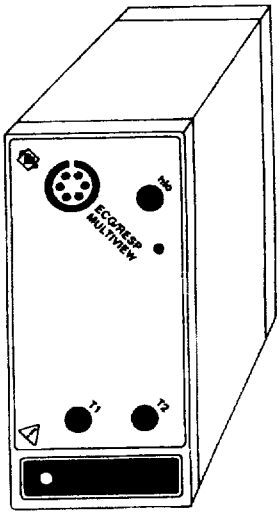
SpaceLabs Medical
The Clinical Information Company



90470



90470-01



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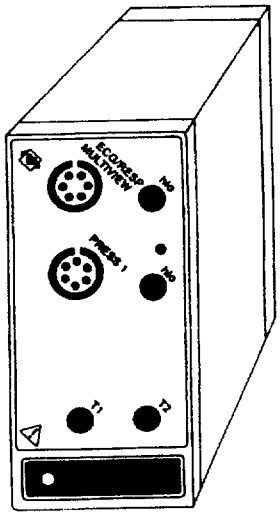


90470-06

Integrated Multi-Parameter Modules 90470 90470-01 90470-02 90470-06

- Touchscreen control of all module functions and compatible with all Patient Care Monitoring System (PCMS™) monitors
- Module Configuration Manager allows hospital to customize module function to specific patient populations, clinical protocols or operating preferences
- Multi-lead ECG with comprehensive arrhythmia and ST analysis and trending options
- Graded alarm function allows the hospital to define different alarm tones (i.e., high, medium or low) according to event severity (critical, warning, advisory)
- Automatic detection of ECG lead fault with user notification; selectable automatic lead switching to maintain monitoring continuity
- Adult and neonatal algorithms

SPECIFICATIONS

Module Configurations —

90470 - Multi-lead ECG, invasive pressure (2 channels), temperature (2 channels)

90470-01 - Multi-lead ECG

90470-02 - Multi-lead ECG, temperature (2 channels)

90470-06 - Multi-lead ECG; invasive pressure (1 channel), temperature (2 channels)

All modules include:

— **Module Configuration Manager** capability (see the *Module Configuration Manager* chapter of the *PCMS Operations Manual* or the *UCW Operations Manual* for complete feature specifications)

— **Basic ECG** alarms for high and low heart rate, asystole and ventricular fibrillation

— **ESIS**

— **Trends** — (with appropriate mainframe option) 24 hours of trended data can be

Integrated Multi-Parameter Modules 90470 90470-01 90470-02 90470-06

SPECIFICATIONS

Data Shuttle™ — (Requires PCMS Monitor Option 20 or UCW Option Q) Includes data transfer features above, plus provides transfer for up to 24 hours of the database of the monitor, including continuous and episodic events, and trend information for all parameters monitored including modules and Flexport® interfaces

Please refer to the appropriate specifications for specific module parameters

ECG

Input Connector — 5-lead or 3-lead ECG cable with AAMI-standard connector (both cables use 1kΩ ± 10% resistors in series with each electrode)

Maximum Input — ± 5 mV (± 10%)

DC Offset — Up to ± 300 mV with no more than 2% signal amplitude degradation

Overdrive Recovery Time — < 1 second circuit settling time with offset voltage < 500 mV

Noise — 30 µV peak-to-peak (RTI) at 100 Hz bandwidth

CMRR — > 110 dB at line frequency (monitor mode) with patient cable and maximum 50 kΩ imbalance (referenced to chassis [earth] ground)

Pacer Rejection — Baseline shift < 0.2 mV (measured at ECG x 1,000 output)

Pacer Detection — Detects pacer pulses of ± 2 mV to ± 700 mV with pulse widths of 0.25 to 2 msec and rise times 10% of width not to exceed 100 µsec

Signal Bandwidth — 0.05 to 100 Hz ± 10% (-3 dB)

Display Bandwidth — 2 settings: 0.5 to 40 Hz ± 10% (-3 dB) in monitor mode, and 0.05 to 70 Hz ± 25% (-3 dB at 50 mm/sec) in extended mode

Sample Rate — 448 Hz

QRS Detection — Performed on up to 2 leads simultaneously; detects QRS complexes with durations of 20 to 120 ms and amplitudes of 0.2 to 5.0 mV (adult) or 0.15 to 5.0 mV (neonatal)

Abnormal Per Minute Counter — Displays counts up to 99 beats per minute

Heart Rate Range — 30 to 300 bpm; heart rates > 300 bpm are displayed as "+++"

Heart Rate Alarm Limits — High: 5 to 300 bpm, Low: 0 to 200 bpm; alarms automatically enabled over a range of 40 (adult) or 100 (neonatal) to 300 bpm

Accuracy — ± 1% or 2 beats per minute (whichever is greater)

Numeric Update Rate — Every 3 seconds or immediately at the onset of an alarm

Test Signal — 1 mV peak-to-peak (displayed via touchkey)

Display Size — Adjustable between 0.5 to 10 cm/mV; users can directly select a size of 1 cm/mV

Displayed Traces — 1 or 2; 2 traces require use of 5-lead patient cable

Trace Sweep Speeds — 50, 25, 12.5 mm per second

High Level Analog Input/Output (front panel) —
Used for defibrillator or intra-aortic balloon pump synchronization
Connector: 0.174" diameter, three conductor TT-phone plug
Dynamic Range: ± 5 mV (± 10%)
Gain: ECG x 1,000 (± 5%)

High Level Analog Output (back panel) —
ECG and Pressure 1 (90470, 90470-06)
ECG and Respiration; if respiration is not available, second output is ECG (90470-01, 90470-02)

ST SEGMENT ANALYSIS

Signal Bandwidth — 0.05 to 100 Hz ± 10% (-3 dB) with mains frequency notch filter

ST Resolution — 8 µV/bit

ST Range — ± 9.20 mm (1 mV = 10 mm)

ST Alarms — Alarms for absolute minimum and maximum ST levels; also changes in ST level over the last 5 minutes

ST Displays — ST values; minimum/maximum/current ST segment deviation and 5-minute averaged segments for the last 30 minutes

ST Measurement Points — Adjustable ST, PR, and J points

ST Trends — Up to 24 hours of trend data can be displayed in 6-, 12- or 24-hour segments

RESPIRATION

Input Connector — 5-lead or 3-lead ECG cable with AAMI-standard connector (both cables use 1K Ω resistors (± 10%) in series with each electrode)

Measurement Technique — Impedance pneumography through ECG leads RA/LA, RL/LL, RL/LA, or RA/LL

Patient Source Impedance — 0 to 1,500 Ω at 62.5 kHz as measured at the patient cable branch

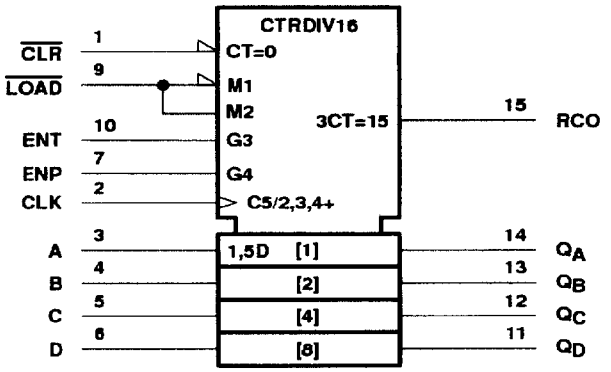
Excitation Frequency — 62.5 kHz (± 1%)

Excitation Amplitude — 80 µAmp (± 20%) RMS, 200 µAmp (± 20%) peak-to-peak

Noise — < 0.05 Ω peak-to-peak at 500 Ωs input source impedance

Signal Bandwidth —
Adult: 0.12 to 2.0 Hz (± 10%)
Neonate: 0.15 to 2.5 Hz (± 10%)

logic symbol†

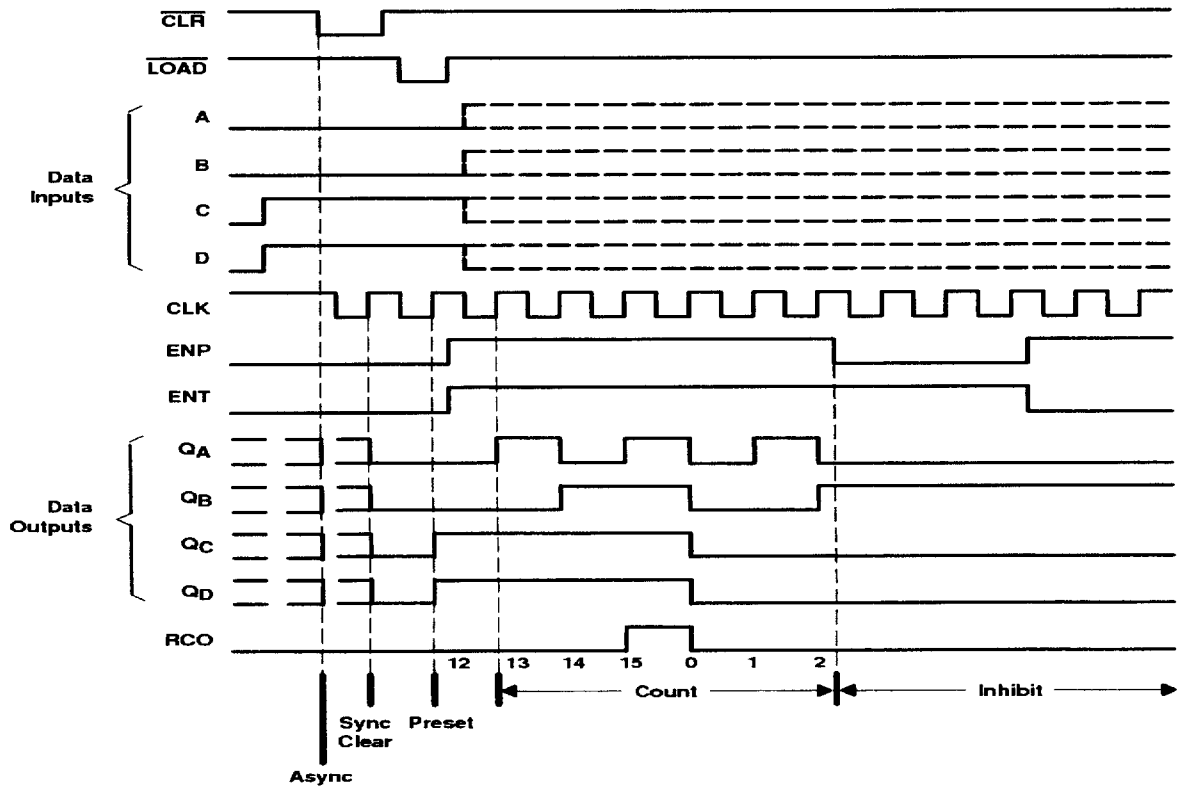


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS124D

January 1998 - Revised September 2003

CD54HC74, CD74HC74, CD54HCT74, CD74HCT74

Dual D Flip-Flop with Set and Reset Positive-Edge Trigger

Features

- **Hysteresis on Clock Inputs for Improved Noise Immunity and Increased Input Rise and Fall Times**
- **Asynchronous Set and Reset**
- **Complementary Outputs**
- **Buffered Inputs**
- **Typical f_{MAX} = 50MHz at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**

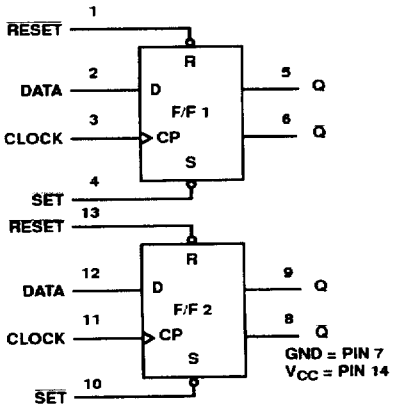
Description

The 'HC74 and 'HCT74 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

This flip-flop has independent DATA, $\overline{SET}$, $\overline{RESET}$ and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The HCT logic family is functionally as well as pin compatible with the standard LS logic family.

Functional Diagram



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H= High Level (Steady State)
L= Low Level (Steady State)
X= Don't Care
↑= Low-to-High Transition
Q0 = the level of Q before the indicated input conditions were established.
NOTE:

1. This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

8-channel analogue multiplexer/demultiplexer

HEF4051B MSI

DESCRIPTION

The HEF4051B is an 8-channel analogue multiplexer/demultiplexer with three address inputs (A_0 to A_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The device contains eight bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by A_0 to A_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 to A_2.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 to A_2, and $\overline{E}$). The V_{DD} to V_{SS} range is 3 to 15 V.

The analogue inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

FUNCTION TABLE

INPUTS				CHANNEL ON
$\overline{E}$	A_2	A_1	A_0	
L	L	L	L	Y_0–Z
L	L	L	H	Y_1–Z
L	L	H	L	Y_2–Z
L	L	H	H	Y_3–Z
L	H	L	L	Y_4–Z
L	H	L	H	Y_5–Z
L	H	H	L	Y_6–Z
L	H	H	H	Y_7–Z
H	X	X	X	none

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial

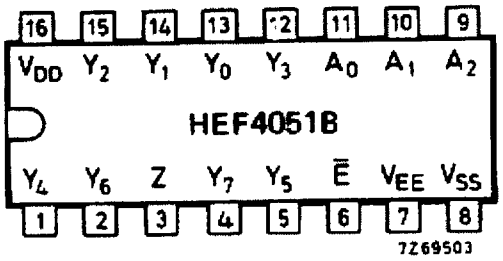


Fig.2 Pinning diagram.

LT1009, LT1009Y
2.5-V INTEGRATED REFERENCE CIRCUITS

description

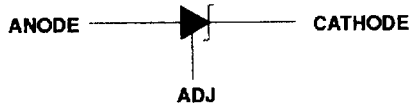
The LT1009 reference circuit is a precision-trimmed 2.5-V shunt regulator featuring low dynamic impedance and a wide operating current range. A maximum initial tolerance of ±5 mV is available in the FK, JG, or LP package and ±10 mV in the D or PK package. The reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient α_{VZ}.

Even though the LT1009 needs no adjustments, a third terminal (ADJ) allows the reference voltage to be adjusted ±5% to eliminate system errors. In many applications, the LT1009 can be used as a terminal-for-terminal replacement for the LM136-2.5, which eliminates the external trim network.

The uses of the LT1009 include a 5-V system reference, an 8-bit ADC and DAC reference, and a power supply monitor. The LT1009 can also be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009C is characterized for operation from 0°C to 70°C. The LT1009I is characterized for operation from −40°C to 85°C. The LT1009M is characterized for operation over the full military temperature range of −55°C to 125°C.

logic symbol



ANALOG DEVICES

LC²MOS
Parallel Loading Dual 12-Bit DAC
AD7547

FEATURES

Two 12-Bit DACs in One Package
DAC Ladder Resistance Matching: 0.5%
Space Saving Skinny DIP and Surface Mount Packages
4-Quadrant Multiplication
Low Gain Error (1LSB max Over Temperature)
Fast Interface Timing

GENERAL DESCRIPTION

The AD7547 contains two 12-bit current output DACs on one monolithic chip. Also on-chip are the level shifters, data registers and control logic for easy microprocessor interfacing. There are 12 data inputs. $\overline{CSA}$, $\overline{CSB}$, $\overline{WR}$ control DAC selection and loading. Data is latched into the DAC registers on the rising edge of $\overline{WR}$. The device is speed compatible with most microprocessors and accepts TTL, 74HC and 5V CMOS logic level inputs.

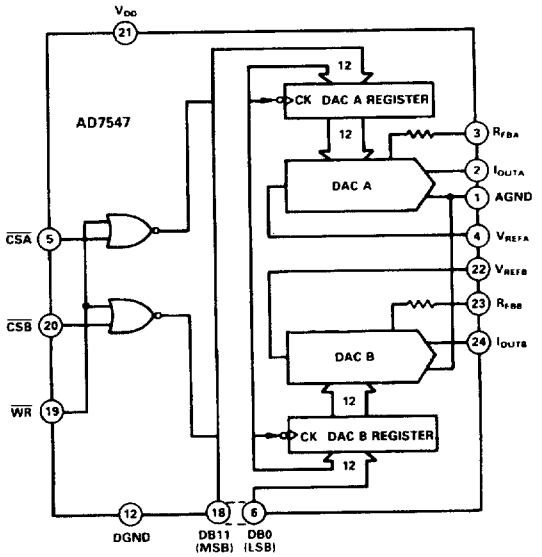
The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Monolithic construction ensures that thermal and gain error tracking is excellent. 12-bit monotonicity is guaranteed for both DACs over the full temperature range.

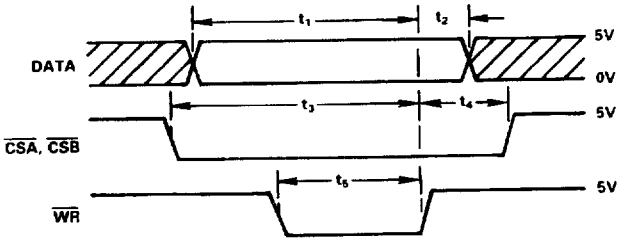
$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC from the Data Bus
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

NOTES
1. X = Don't care
2. ↓ means rising edge triggered

Table I. AD7547 Truth Table

FUNCTIONAL BLOCK DIAGRAM





NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH}+V_{IL}}{2}$

Figure 1. Timing Diagram for AD7547

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation.

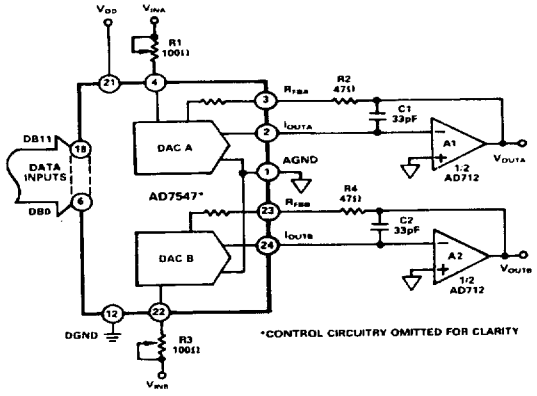


Figure 4. AD7547 Unipolar Binary Operation

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5.

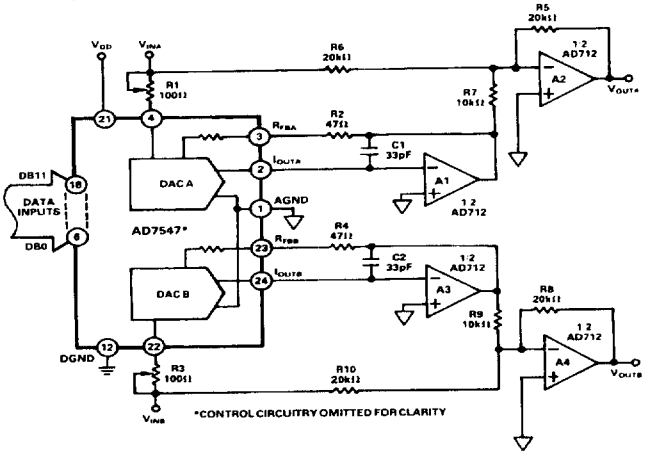
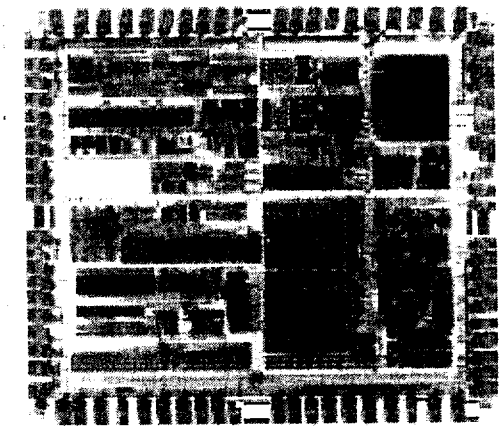


Figure 5. Bipolar Operation (Offset Binary Coding)

80C186XL/80C188XL
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSORS

- **Low Power, Fully Static Versions of 80C186/80C188**
- **Operation Modes:**
  - **Enhanced Mode**
    - **DRAM Refresh Control Unit**
    - **Power-Save Mode**
    - **Direct Interface to 80C187 (80C186XL Only)**
  - **Compatible Mode**
    - **NMOS 80186/80188 Pin-for-Pin Replacement for Non-Numerics Applications**
- **Integrated Feature Set**
  - **Static, Modular CPU**
  - **Clock Generator**
  - **2 Independent DMA Channels**
  - **Programmable Interrupt Controller**
  - **3 Programmable 16-Bit Timers**
  - **Dynamic RAM Refresh Control Unit**
  - **Programmable Memory and Peripheral Chip Select Logic**
  - **Programmable Wait State Generator**
  - **Local Bus Controller**
  - **Power-Save Mode**
  - **System-Level Testing Support (High Impedance Test Mode)**
- **Completely Object Code Compatible with Existing 8086/8088 Software and Has 10 Additional Instructions over 8086/8088**
- **Speed Versions Available**
  - **25 MHz (80C186XL25/80C188XL25)**
  - **20 MHz (80C186XL20/80C188XL20)**
  - **12 MHz (80C186XL12/80C188XL12)**
- **Direct Addressing Capability to 1 MByte Memory and 64 Kbyte I/O**
- **Available in 68-Pin:**
  - **Plastic Leaded Chip Carrier (PLCC)**
  - **Ceramic Pin Grid Array (PGA)**
  - **Ceramic Leadless Chip Carrier (JEDEC A Package)**
- **Available in 80-Pin:**
  - **Quad Flat Pack (EIAJ)**
  - **Shrink Quad Flat Pack (SGFP)**
- **Available in Extended Temperature Range (−40°C to +85°C)**

The Intel 80C186XL is a Modular Core re-implementation of the 80C186 microprocessor. It offers higher speed and lower power consumption than the standard 80C186 but maintains 100% clock-for-clock functional compatibility. Packaging and pinout are also identical.



272431-1

June, 2002 Order Number: 272431-005