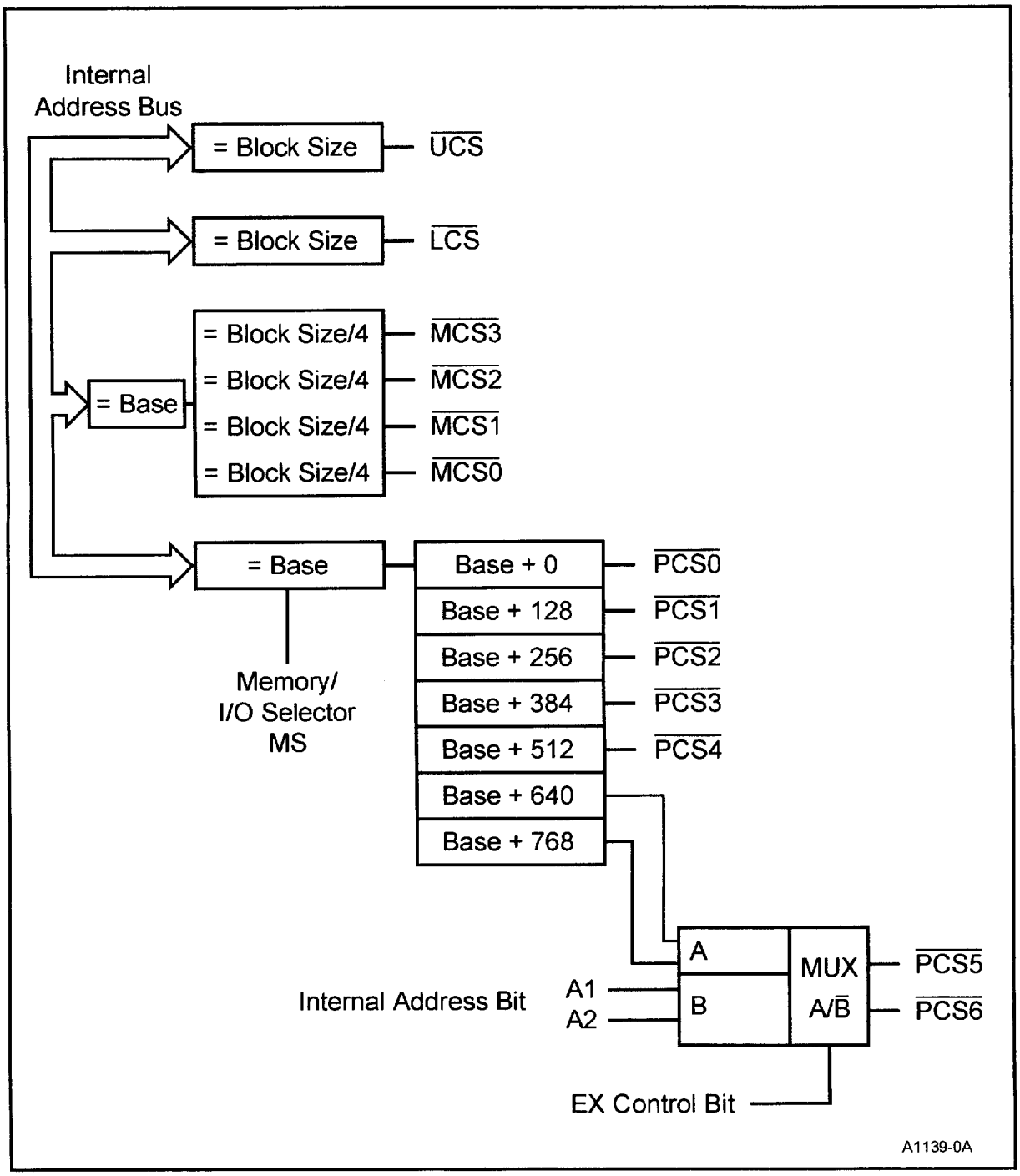


Figure 6-2. Chip-Select Block Diagram

$\overline{UCS}$ Mapped only to the upper memory address space; selects the BOOT memory device (EPROM or Flash memory types).

$\overline{LCS}$ Mapped only to the lower memory address space; selects a static memory (SRAM) device that stores the interrupt vector table, local stack, local data, and scratch pad data.

$\overline{MCS3:0}$ Mapped only to memory address space; selects additional SRAM memory, DRAM memory, or the system bus.

$\overline{PCS6:0}$ Mapped to memory or I/O address space; selects peripheral devices or generates a DMA acknowledge strobe. Note that each PCS*x* is not individually configurable for I/O space or memory space.

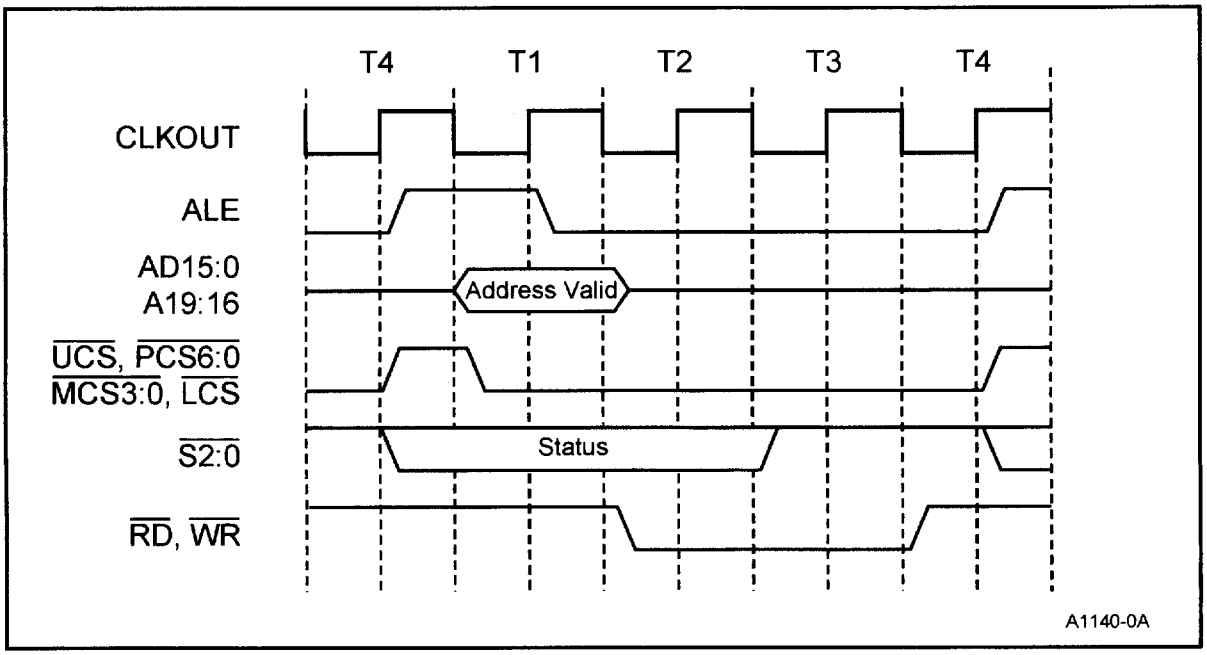


Figure 6-3. Chip-Select Relative Timings

The $\overline{UCS}$ chip-select always ends at address location 0FFFFH; its block size (and thus its starting address) is programmed in the UMCS register (Figure 6-5 on page 6-7). The $\overline{LCS}$ chip-select always starts at address location 0H; its block size (and thus its ending address) is programmed in the LMCS Control register (Figure 6-6 on page 6-8). The block size can range from 1 Kbyte to 256 Kbytes for both.

The $\overline{MCS3:0}$ chip-selects access a contiguous block of memory address space. The block size can range from 8 Kbytes to 512 Kbytes; it is programmed in the MMCS register (Figure 6-7 on page 6-9). Each chip-select goes active for one-fourth of the block. The start address is programmed in the MPCS register (Figure 6-9 on page 6-11); it must be an integer multiple of the block size. Because of the start address limitation, the $\overline{MCS3:0}$ chip-selects cannot cover the entire memory address space between the $\overline{LCS}$ and $\overline{UCS}$ chip-selects.

Table C-4. Instruction Set (Continued)

Name	Description	Operation	Flags Affected

MOV	**Move (Byte or Word):**
	MOV *dest, src*
	Transfers a byte or a word from the source operand to the destination operand.
	Instruction Operands:
	MOV mem, accum
	MOV accum, mem
	MOV reg, reg
	MOV reg, mem
	MOV mem, reg
	MOV reg, immed
	MOV mem, immed
	MOV seg-reg, reg16
	MOV seg-reg, mem16
	MOV reg16, seg-reg
	MOV mem16, seg-reg
		(dest)←(src)	AF –
			CF –
			DF –
			IF –
			OF –
			PF –
			SF –
			TF –
			ZF –

OUT	**Output:** OUT *port, accumulator* Transfers a byte or a word from the AL register or the AX register, respectively, to an output port. The port number may be specified either with an immediate byte constant, allowing access to ports numbered 0 through 255, or with a number previously placed in register DX, allowing variable access (by changing the value in DX) to ports numbered from 0 through 65,535. **Instruction Operands:** OUT immed8, AL OUT DX, AX	(dest) ← (src)	AF – CF – DF – IF – OF – PF – SF – TF – ZF –

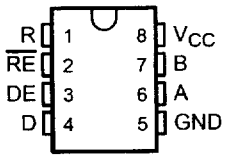
NOTE: The three symbols used in the Flags Affected column are defined as follows:
– the contents of the flag remain unchanged after the instruction is executed
? the contents of the flag is undefined after the instruction is executed
✓the flag is updated after the instruction is executed

Bitwise Operator Overview of the compilator

Operator	Operation	Operator	Operation
&	bitwise AND; compares pairs of bits and returns 1 if both bits are 1, otherwise returns 0	~	bitwise complement (unary); inverts each bit
|	bitwise (inclusive) OR; compares pairs of bits and returns 1 if either or both bits are 1, otherwise returns 0	<<	bitwise shift left; moves the bits to the left, discards the far left bit and assigns 0 to the right most bit.
^	bitwise exclusive OR (XOR); compares pairs of bits and returns 1 if the bits are complementary, otherwise returns 0	>>	bitwise shift right; moves the bits to the right, discards the far right bit and if unsigned assigns 0 to the left most bit, otherwise sign extends

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and ITU Recommendation V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements

D OR P PACKAGE
(TOP VIEW)



description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

Function Tables

DRIVER

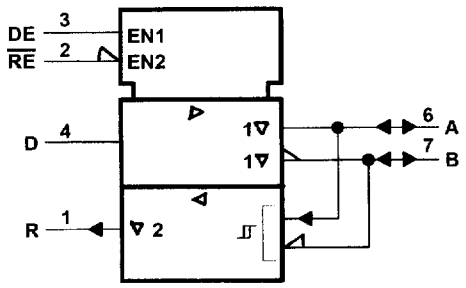
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

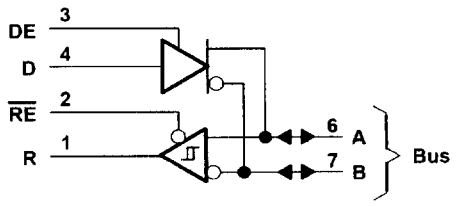
DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	?

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Le protocole SDLC (Synchronous Data Link Control)

Ce protocole est destiné à des réseaux multi-périphériques, chaque périphérique étant repéré par une adresse unique.

Il est de type synchrone, l'horloge qui rythme l'émission des données est transmise sur un autre conducteur que les données.

Format de la trame SDLC

Une trame est une suite d'octets organisés en champs.

Longueur des champs en octet	1	1	1	variable	2	1
Nom des champs	**Drapeau**	**Adresse du destinataire**	**Commande**	**Données**	**FCS**	**Drapeau**

La partie utile (sans les drapeaux) de la trame SDLC a une longueur variable mais comprise entre 32 bits (4 octets) minimum et 1150 bits maximum. Cette partie utile est encadrée par des drapeaux qui indiquent le début et la fin de la trame.

Les différents champs sont toujours transmis poids faibles en premier, poids forts en dernier.

Contenu des différents champs

- Les **drapeaux** permettent au système de réception de reconnaître le début et la fin de la trame. Ils sont constitués de l'octet **01111110** (un 0 suivi de six 1 suivi d'un 0). Cela implique que dans le reste du message on ne pourra pas transmettre plus de cinq 1 consécutifs.

- **Adresse du destinataire :** contient l'adresse du périphérique auquel est destiné la commande ou les données

L'adresse « broadcast » $(11111111)_2$ ou $(FF)_{16}$ est utilisée pour transmettre un message à tous les périphériques.

- **Commande :** Ce champ indique le type de la trame (information, supervision ou non numéroté) et le numéro de la trame émise ou à recevoir.

- **Données :** Ce champ, lorsqu'il est présent, contient les données à transmettre entre les périphériques.Il peut être, lui-même, organisé à un niveau supérieur.

- **Frame Check Sequence (FCS) :** Ce champ permet au périphérique récepteur de détecter une erreur de transmission; il peut alors demander une retransmission des trames erronées.

Les bits de transparence

Pour qu'une succession de six 1 ne se produise que dans les drapeaux, on insère dans le reste de la trame un 0 après chaque suite de cinq 1. Ces bits supplémentaires sont éliminés par le récepteur.

Exemple : la portion de message 000111001111111000011111111111100000011 devient 000111001111101100001111101111010000011 par insertion automatique des 0 notés en gras.

IA8044/IA8344 Data Sheet
SDLC COMMUNICATIONS CONTROLLER

FEATURES

Form, Fit, and Function Compatible with the Intel® 8044/8344

Packaging options available: 40 Pin Plastic Dual In-Line Package (PDIP), 44 Pin Plastic Leaded Chip Carrier (PLCC)

8-Bit Control Unit

8-Bit Arithmetic-Logic Unit with 16-Bit multiplication and division

12 MHz clock

Four 8-Bit Input / Output ports

Two 16-Bit Timer/Counters

Serial Interface Unit with SDLC/HDLC compatibility

2.4 Mbps maximum serial data rate

Two Level Priority Interrupt System

5 Interrupt Sources

Internal Clock prescaler and Phase generator

192 Bytes of Read/Write Data Memory Space

64kB External Program Memory Space

64kB External Data Memory Space

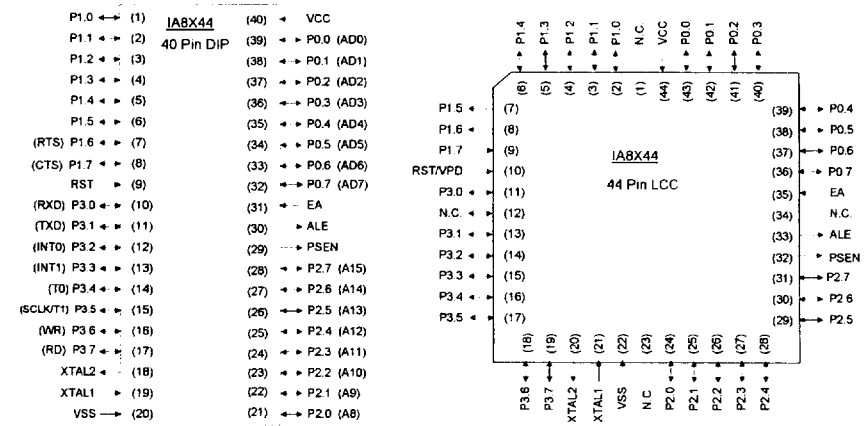
4kB Internal ROM (IA8044 only)

IA8044/IA8344 Variants

IA8044	4kB internal ROM with R0117 version 2.3 firmware, 192 byte internal RAM, 64kB external program and data space.
IA8344	192 byte internal RAM, 64kB external program and data space.

The IA8044/IA8344 is a "plug-and-play" drop-in replacement for the original IC. InnovASIC produces replacement ICs using its MILESTM, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILESTM captures the design of a clone so it can be produced even as silicon technology advances. MILESTM also verifies the clone against the original IC so that even the "undocumented features" are duplicated. This data sheet documents all necessary engineering information about the IA8044/IA8344 including functional and I/O descriptions, electrical characteristics, and applicable timing.

Package Pinout



I/O Characteristics

The table below describes the I/O characteristics for each signal on the IC. The signal names correspond to the signal names on the pinout diagrams provided. The table below provides the I/O description of the IA8044 and the IA8344.

Name	Type	Description
RST	I	Reset. This pin when held high for two machine cycles while the oscillator is running will cause the chip to reset.
ALE	O	Address Latch Enable. Used to latch the address on the falling edge for external memory accesses.
PSEN	O	Program Store Enable. When low acts as an output enable for external program memory.
EA	I	External Access. When held low EA will cause the IA8044/IA8344 to fetch instructions from external memory.
P0.7 – P0.0	I/O	Port 0. 8 bit I/O port and low order multiplexed address/data byte for external accesses.
P1.7 – P1.0	I/O	Port 1. 8-bit I/O port. Two bits have alternate functions, P1.6 (RTS) and P1.7 (CTS).
P2.7 – P2.0	I/O	Port 2. 8-bit I/O port. It also functions as the high order address byte during external accesses.
P3.7 – P3.0	I/O	Port 3. 8-bit I/O port. Port 3 bits also have alternate functions as described below. P3.0 – RXD. Receive data input for SIU or direction control for P3.1 dependent upon datalink configuration. P3.1 – TXD. Transmit data output for SIU or data input/output dependent upon datalink configuration. Also enables diagnostic mode when cleared. P3.2 – INT0. Interrupt 0 input or gate control input for counter 0. P3.3 – INT1. Interrupt 1 input or gate control input for counter 1. P3.4 – T0. Input to counter 0. P3.5 – SCLK/T1. SCLK input to SIU or input to counter 1. P3.6 – WR. External memory write signal. P3.7 – RD. External memory read signal.
XTAL1	I	Crystal Input 1. Connect to VSS when external clock is used on XTAL2. May be connected to a crystal (with XTAL2), or may be driven directly with a clock source (XTAL2 not connected).
XTAL2	O	Crystal Input 2. May be connected to a crystal (with XTAL1), or may be driven directly with an inverted clock source (XTAL1 tied to ground).
VSS	P	Ground.
VCC	P	+5V power.

Interrupts Vectors

Location	Service
0003H	External Interrupt 0
000BH	Timer 0 overflow
0013H	External Interrupt 1
001BH	Timer 1 overflow
0023H	SIU Interrupt

Timers/Counters

Timers 0 and 1

The IA8X44 has two 16-bit timer/counter registers: Timer 0 and Timer 1. Both can be configured for counter or timer operations. In timer mode, the register is incremented every machine cycle, which means that it counts up after every 12 oscillator periods. In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle (12 clock periods). Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

Mode 0

In mode 0 the timers operate as an 8-bit timer (TH0/1) with a divide by 32 bit prescalar (TL0/1). Mode 0 uses all 8 bits of TH0/1 and the lower 5 bits of TL0/1. The upper 3 bits of TL0/1 are unknowns. Setting TR0/1 does not reset the registers TH0/1 and TL0/1. As the timer rolls over from all 1's to all 0's it will set the interrupt flag TF0/1.

Mode 1

Mode 1 is the same as mode 0 except that all 8 bits of TL0/1 are used instead of just the lower 5 bits.

Mode 2

Mode 2 configures TL0/1 as an 8-bit counter with automatic reload from the contents of TH0/1. Overflow of TL0/1 causes the interrupt TF0/1 to be set and the reload to occur. The contents of TH0/1 are not affected by the reload.

Mode 3

Mode 3 creates two separate 8 bit counters from TL0 and TH0. TL0 uses the timer 0 mode bits from TMOD, TMOD.0 through TMOD.3. TH0 is a timer only (not a counter) and uses timer 1's control bits, TR1 and TF1 for operation. Timer 1 can still be used if an interrupt is not required by switching it in and out of its own mode 3. With TMOD.4 and TMOD.5 both high timer 1 will stop and hold its count.

Timer Mode (TMOD):

The Timer Mode register contains bits that select the mode that the timers are to be operated in. The lower nibble controls timer 0 and the upper nibble controls timer 1.

TMOD

Bit : 7	6	5	4	3	2	1	0
GATE	C/T	M1	M0	GATE	C/T	M1	M0

TMOD.0	M0	Timer 0 mode selector bit.
TMOD.1	M1	Timer 0 mode selector bit.
TMOD.2	C/T	C/T Selects Timer0 or Counter0 operation. When set to 1, the Counter operation is performed, when cleared to 0, the register will function as a Timer.
TMOD.3	GATE	If set, enables external gate control for counter/timer0 (pin INT0/ for Counter 0). When INT0/ is high, and TR0 bit is set (see TCON register), the counter is incremented every falling edge on T0 input pin.
TMOD.4	M0	Timer 1 mode selector bit.
TMOD.5	M1	Timer 1 mode selector bit.
TMOD.6	C/T	C/T Selects Timer1 or Counter1 operation. When set to 1, the Counter operation is performed, when cleared to 0, the register will function as a Timer.
TMOD.7	GATE	If set, enables external gate control for counter/timer1 (pin INT1/ for Counter 1). When INT1/ is high, and TR1 bit is set (see TCON register), the counter is incremented every falling edge on T1 input pin.

Timer Mode Select Bits

M1	M0	Operating Mode	
0	0	0	13 bit timer
0	1	1	16 bit timer/counter
1	0	2	8 bit auto-reload timer/counter
1	1	3	Timer0 – TL0 is a standard 8-bit timer/counter controlled by timer 0 control bits. TH0 is an 8-bit timer function only, controlled by timer 1 control bits.
1	1	3	Timer/counter1 stopped and holds its count. Can be used to start/stop timer 1 when timer 0 is in mode 3.

Timer Control (TCON):

The Timer Control register provides control bits that start and stop the counters. It also contains bits to select the type of external interrupt desired, edge or level. Additionally TCON contains status bits showing when a timer overflows and when an interrupt edge has been detected.

TCON

Bit : 7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TCON.0	IT0	Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.
TCON.1	IE0	Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT1/ is observed. Cleared when interrupt is processed.
TCON.2	IT1	Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.
TCON.3	IE1	Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1/ is observed Cleared when interrupt is processed.
TCON.4	TR0	Timer 0 Run control bit. If cleared, Timer 0 stops.
TCON.5	TF0	Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag should be cleared by software.
TCON.6	TR1	Timer 1 Run control bit. If cleared, Timer 1 stops. In mode 3 this bit controls TH0.
TCON.7	TF1	Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag should be cleared by software.. In mode 3 this bit is controlled by TH0.

Timers/Counters Configuration

Timer 0 Mode 2