BREVET DE TECHNICIEN SUPERIEUR

SYSTÈMES ÉLECTRONIQUES

ÉPREUVE E4
Étude d'un Système Technique

Unité E4-1
ÉLECTRONIQUE

Durée : 4 heures — coefficient : 4

Tout document interdit

Calculatrice à fonctionnement autonome autorisée
(Circulaire 99-186 du 16/11/99)

Ce sujet comporte :

A- Analyse fonctionnelle du système :	A1 à A7
B- Sujet:	
Questionnaire :	B1 à B5
Documents réponse :	BR1 à BR6
Documentation	BAN1 à BAN20

ANALYSE FONCTIONNELLE

Présentation du système Station d'alerte, support de l'étude

1-1 Mise en situation

Dans les pays industrialisés, les problèmes de sécurité constituent une préoccupation majeure. Pour le distributeur d'eau, cette préoccupation se traduit par la nécessité de fournir à ses abonnés une eau en tout point conforme aux normes de potabilité en vigueur.

Par définition, une eau potable est une eau agréable à boire et sans danger pour le consommateur. La législation précise cette définition par des normes de potabilité concernant :

- la teneur en organismes parasites ou pathogènes,
- la coloration,
- la turbidité (< 2NTU),
- la minéralisation (< 2g/l),
- la teneur en métaux lourds (plomb, cuivre, manganèse ...),
- la teneur en produits chimiques toxiques (arsenic, cyanures, fluorures ...).

Les eaux auxquelles l'on a recours pour l'alimentation publique ne répondent généralement pas à ces normes et doivent donc être traitées avant distribution. Par ailleurs, chaque eau possède des caractéristiques propres. Une analyse de l'eau brute est indispensable afin d'adapter le traitement à la qualité de l'eau. En cas de pollution accidentelle, il faut pouvoir arrêter le pompage de l'eau brute afin de ne pas contaminer les réserves en eau potable. Une station d'alerte répond à ce besoin et constitue un système de surveillance automatique de la qualité de l'eau.

L'objet technique étudié est un turbidimètre. Cet appareil mesure en continu la turbidité de l'eau brute au sein de la station d'alerte. La turbidité est définie comme l'expression de la diffusion et de l'absorption (par opposition à la transmission) de la lumière au travers d'un échantillon d'eau. Elle est provoquée par la présence de particules en suspension (colloïdes, algues, microorganismes, argile....). Le taux de lumière diffusé et absorbé est proportionnel à la concentration en particules dans la solution.

La turbidité est un indicateur relativement fiable de la pureté d'une solution et s'exprime en Nephelometric Turbidity Units (NTU).

Cette mesure de la turbidité permet d'optimiser la durée de la filtration de l'eau brute. Des seuils de turbidité ont été fixés pour modifier cette durée de filtration en cas de dépassement.

1-2Principe et procédé de la mesure

Principe de mesure

La mesure de la turbidité peut être effectuée de deux manières :

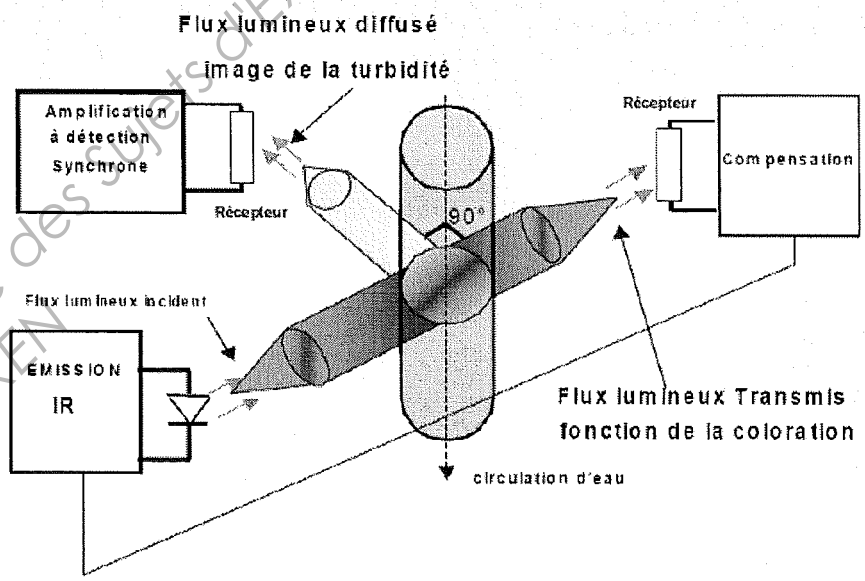
- soit par la mesure de la lumière qui traverse le liquide en ligne droite. C'est la turbidimétrie. Cette méthode est appliquée seulement aux liquides dont la coloration ne change pas,
- soit par la mesure de la lumière diffusée par les particules en suspension dans un axe différent de celui de la source de lumière. En effet, les particules en suspension et elles seules réfléchissent la lumière dans toutes les directions. Ce principe de mesure est appelé Néphélométrie du grec NEPHELE (« nuage »). La coloration du liquide n'entraîne aucune diffusion de lumière mais seulement une atténuation de celle-ci. Il faut, alors, réguler l'intensité de la lumière émise en fonction de la coloration. Lorsque la coloration est importante, il faut donc augmenter l'intensité de la lumière. C'est ce second principe qui est utilisé dans le turbidimètre « Turbilight ».

Procédé de mesure

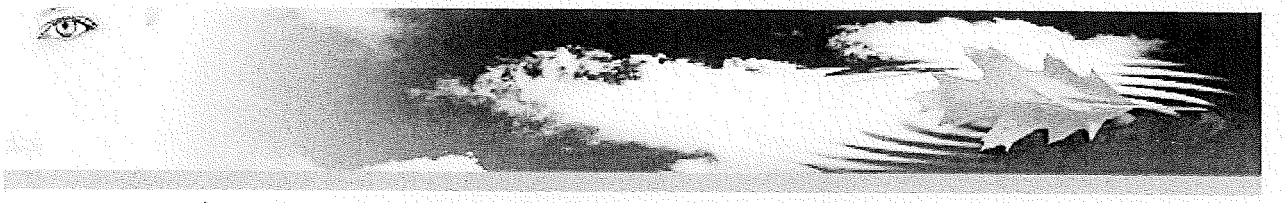
Un faisceau infrarouge, de fréquence F0, issu d'une DEL va traverser une cuve de mesure qui contient l'échantillon. L'intensité de la lumière diffusée est mesurée à 90 degrés du rayon incident par un récepteur puis amplifiée électroniquement.

À partir de l'intensité diffusée par l'échantillon et d'une référence de turbidité connue (étalonnage) pour la plage de mesure utilisée, l'appareil va calculer la turbidité de l'échantillon. Les références d'étalonnage sont des liquides purs (eau de Volvic = 0,06NTU) ou des suspensions stables de Formazine de turbidité connue.

Une mesure à 180 degrés est également effectuée pour compenser l'atténuation due au vieillissement de la DEL et à la couleur de l'eau.

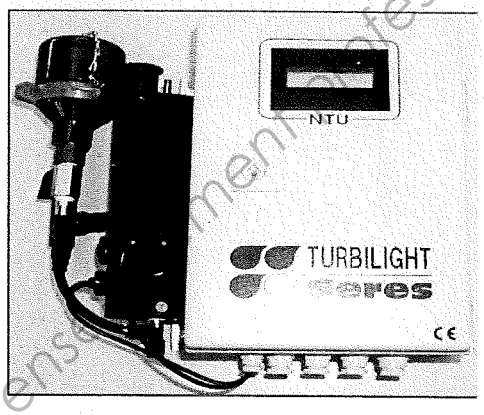


1-3 Caractéristiques du Turbilight



TURBILIGHT

Low & Medium RangesTurbidity Water Monitor



PRINCIPLE & BACKGROUND

The SERES environnement TURBILIGHT is dedicated to the continuous measurement of low turbidities in water using the nephelometric method.

The excellent performances demonstrated by the TURBILIGHT rely on its characteristics :

- Resolution, i.e. the ability of an instrument to detect any measured value variation :
  - 0.01 NTU resolution for a 30 s integration time
  - 0.001 NTU resolution for a 2 mn integration time
  - no idle time
- Repeatability , that corresponds to the variation between two separate measurements made on the same sample :
  - repeatability of ± 1% of full range
- Accuracy, that depends on the exactness of calibration and reapeatability :
  - upon factory calibration, accuracy is ± 1% of full range.

Due to the uncertainty around calibration on-site, resolution is in fact the most important parameter in an auto-controlled operation.

- Base line background noise is < 0.001 NTU
- Perfect linearity of the signal, without interference for high turbidity values, on 0 - 10 NTU range.
- Drift : no drift over a 2-week period with 50 NTU suspended particles

FEATURES

- Conforms to ISO 7027 / NF EN 27027 standards.
- Nephelometric measurement
- IR source (LED) at 850 nm ± 20 nm
  Life time exceeding 3 years
- Collimated incident beam
- 90° measuring angle with a reduced optical path to prevent interferent reflections.
- Compensation of light source ageing and of water colour achieved via a measurement at 180°.

Convenient installation, operation and service :

- Compact, portable device
- 230 VAC or 24 VDC power supply (standard)
- Automatic cleaning of cell walls at programmable frequency.
- Routine calibration once every 6 months

APPLICATIONS

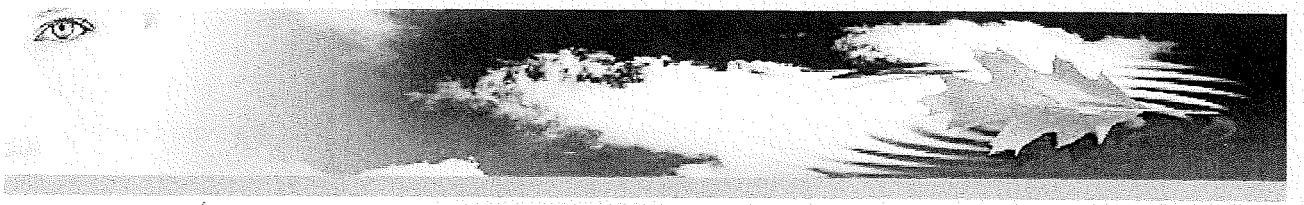
Continuous follow-up of the quality of :

- drinking water,
- surface water.

Low & medium ranges : from 0-2 to 0-1000 NTU

www.seres-france.com

SERES environnement



TURBILIGHT

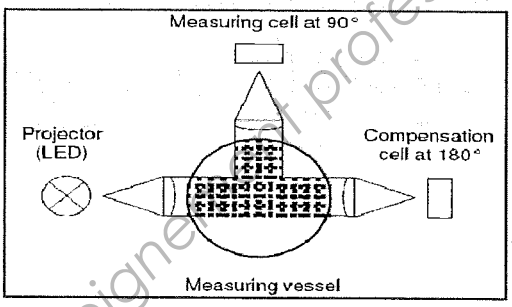
ANALYTICAL METHOD

The TURBILIGHT operates on the principle of nephelometry that consists in measuring light diffused at an angle of 90 degrees to that of an incident light beam.

The resulting signal is strictly proportional to the concentration of diffusing particles and to the water turbidity.

The zero is "true". There is no signal if the measuring vessel contains turbidity-free water.

The measuring vessel is pressurized to eliminate air bubbles interferences.



TECHNICAL SPECIFICATIONS

Measuring ranges :	Low 0-2 NTU - 0-5 NTU - 0-10 NTU 0-20 NTU - 0-50 NTU - 0-100 NTU Medium 0-100 NTU - 0-250 NTU - 0-500 NTU 0-750 NTU - 0-1000 NTU Ranges are user configurable and selectable
Measuring units :	NTU or FTU (others on request)
Measurement :	continuous
Response time :	initial response : few seconds 90% of value within less than 30 seconds
Accuracy :	± 1% full range
Resolution :	0,001 NTU for full range 0-5 NTU
Repeatability :	± 1% full range
Calibration :	Manual using 2 standard solutions (slope and zero) (once every 6 months)
Hydraulic supply :	50 l/h approx. 6 bars maximum
Sample temperature :	4°C minimum / 40°C maximum
Cleaning :	basic unit with automatic system using a piston operated wiper at 10 min or user configured frequency
Display :	1 line alphanumerical - 8 characters
Output signal :	. 0-20 mA or 4-20 mA (500 ohms) . RS232 current loop by interface converter (option) . JBUS / RS485 signal (option)
Alarms :	. 2 thresholds per dry contact relay (programmable) . analyser failure
Electric power supply :	230V AC – 50 Hz or 24V DC - 25W (110 V AC—60 Hz option)
EMC certified :	NF EN610004-2 CEI 801-2 NF EN610004-4 CEI 801-4 NF C 46-022 CEI 801-3 NF EN55022
Dimensions & weight :	Steel epoxy IP65 housing 300 x 340 x 150 mm (H x L x W) Weight : 6.5 kg

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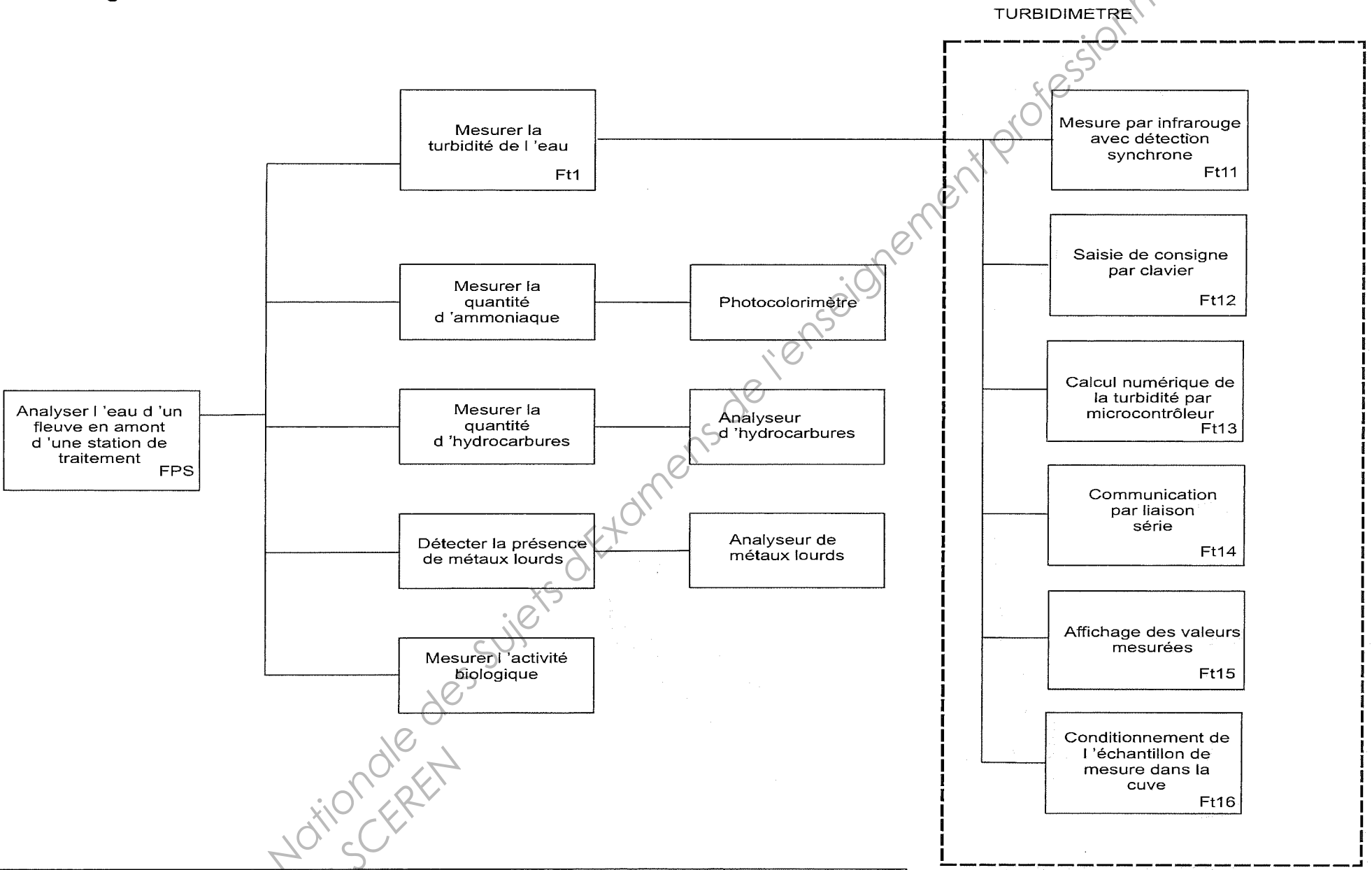
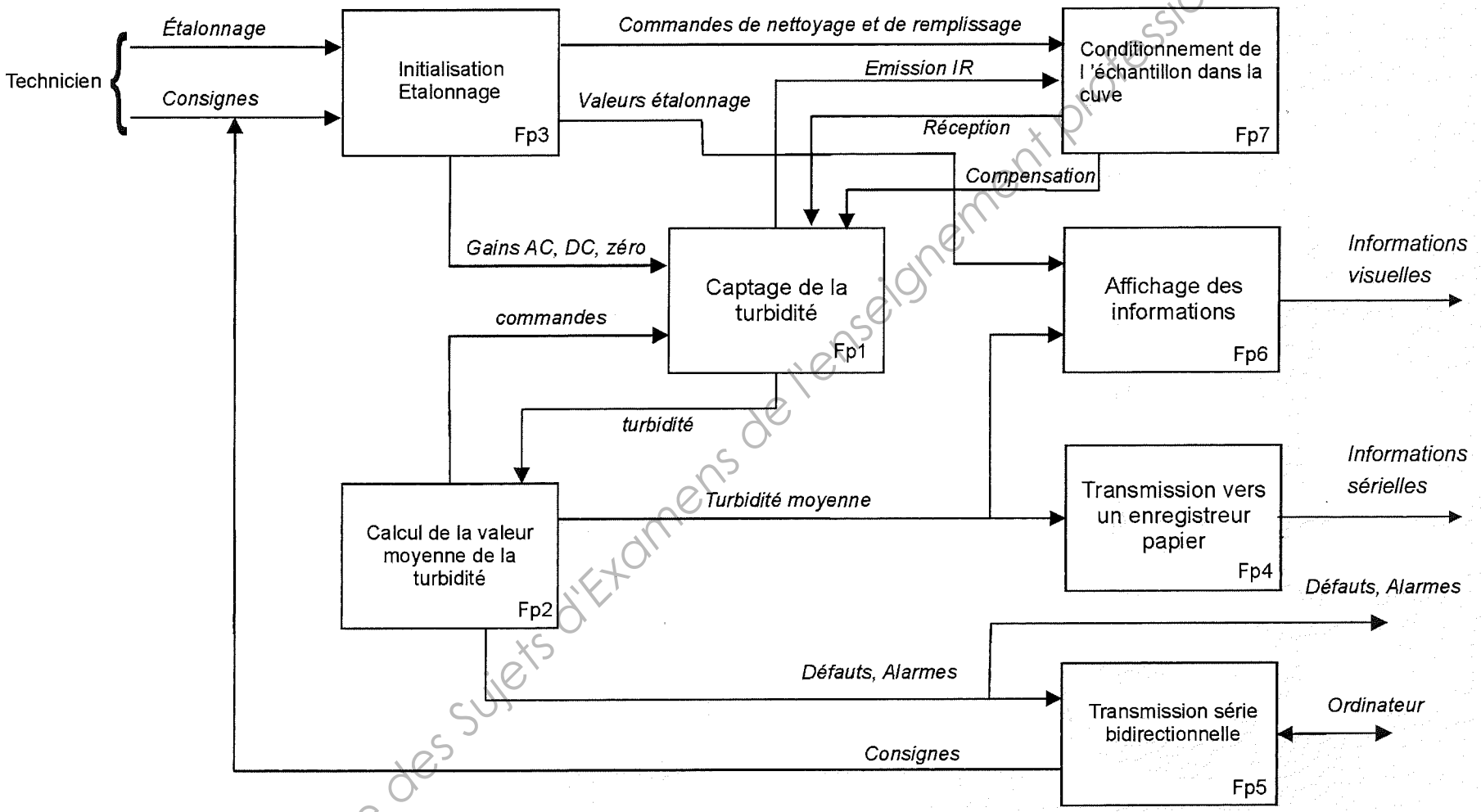
SERES environnement

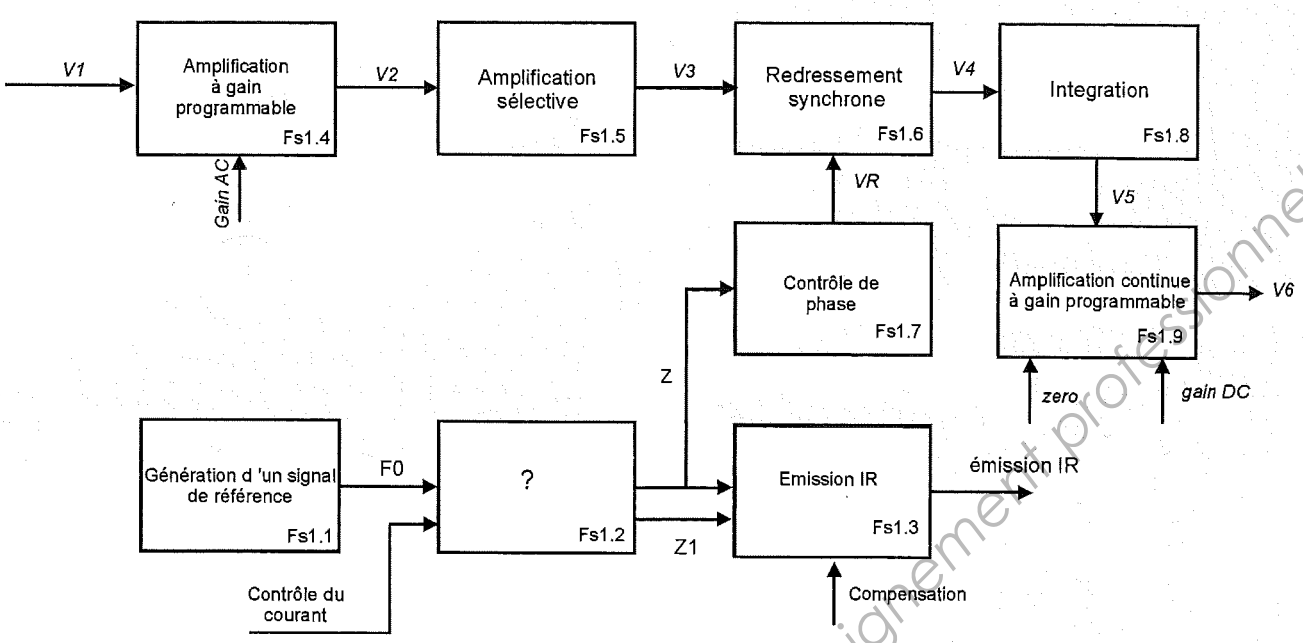
1-4 Diagramme FAST de la station d'alerte



1-5 Schéma fonctionnel de 1er degré du turbidimètre



1-6Schéma fonctionnel du second degré FP1



Remarque : les fonctions secondaires Fs1.5 à Fs1.9 ne seront pas étudiées.

- **Fs1.1 Génération d'un signal de référence**

Sortie :

F0 : signal binaire de fréquence F0.

- **Fs1.2 à définir**

- **Fs1.3 Émission IR (voir BAN19)**

La compensation contrôle le courant de la DEL émettrice D1 (donc l'intensité du flux lumineux émis) en commandant le transistor T4 en régime linéaire à partir de la mesure du flux lumineux traversant la cuve de mesure et de l'écart entre la valeur mesurée et une valeur de consigne.

Par ailleurs, le flux lumineux émis est haché par le transistor T5 à partir du signal de commande de découpage Z.

Enfin le signal Z1venat du microcontrôleur (P2.5) permet de limiter le courant dans la DEL émettrice pendant la phase de démarrage de la compensation, le transistor T3 étant alors saturé.

Entrées :

Z : signal rectangulaire de rapport cyclique ½ et de fréquence F0 qui sera utilisé pour le découpage du flux IR et servira de référence pour la détection synchrone,

Z1 : signal de commande envoyé par l'unité centrale pour limiter le courant dans le DEL durant la phase de démarrage de la compensation,

Compensation : signal analogique permettant la commande en régime linéaire de T4.

Sortie :

Émission IR : Flux IR émis de rapport cyclique ½ et de fréquence F0 dont l'amplitude est contrôlée par la compensation.

- **Fs1.4 amplification à gain programmable**

Entrées :

V1 : tension alternative de fréquence F0 possédant une composante continue, dont l'amplitude est proportionnelle à la turbidité.

Gain AC : signal binaire permettant de modifier le gain.

Sortie :

V2 : tension alternative de fréquence F0.

SUJET

Les trois parties du sujet sont indépendantes. Les réponses aux questions sont à rendre sur feuilles d'examen. Les documents réponse sont à rendre dans tous les cas avec votre copie même si vous n'y avez pas répondu.

Partie A Analyse fonctionnelle

Q1. Préciser l'intérêt d'une station d'alerte.

Q2. Citer les différents appareils qui permettent d'évaluer l'état de pollution de l'eau avant traitement.

Q3. Citer le paramètre de nettoyage qui sera modifié dans la centrale de contrôle si la mesure de la turbidité de l'eau brute dépasse les seuils.

Q4. Décrire brièvement le processus de mesure utilisé dans le turbidimètre « Turbilight ».

Q5. Expliquer comment une forte coloration de l'eau (boue, petite pollution...) ne perturbe pas la fiabilité de la mesure.

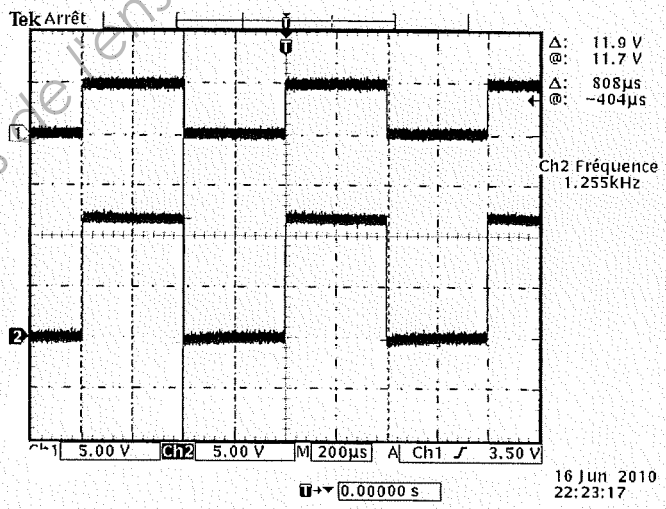
Q6. Indiquer la gamme de mesure maximale et la précision du turbidimètre « Turbilight ».

PARTIE B Captage de la turbidité FP1 « émission IR »

1. Emission infrarouge FS1.3

Voir schéma strùcturel BAN19

On donne ci-contre les chronogrammes des signaux Fo (repère 1) et Z (repère 2).



Q7. A partir des chronogrammes ci-contre et de la documentation technique BAN2, calculer la fréquence du quartz du circuit CI7

Q8. Indiquer le rôle de la fonction Fs1.2.
Justifier sa présence.
Entourer sur le schéma structurel (doc réponse BR1) la structure qui remplie ce rôle.

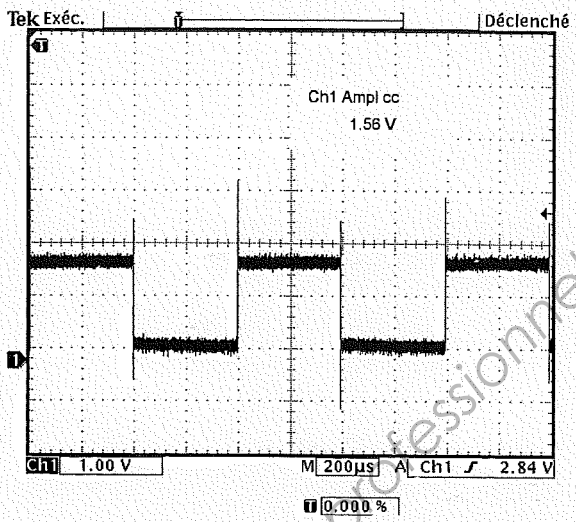
Q9. Nommer la fonction Fs1.2 dans le schéma fonctionnel (doc réponse BR2).

Q10. Déterminer les états des transistors T3 et T5 en fonction des niveaux de tensions présents en Z et Z1 dans le document réponse BR2.

Q11. Compléter le tableau document réponse BR2 :

- en dessinant les modèles équivalents des deux transistors,
- en donnant l'état de la DEL IR DE1 lorsque T4 conduit.

Q12. A partir du chronogramme ci-contre issu du point test Pt1 image du courant dans la DEL DE1 avec la tension au point Z1 égale à +12V, calculer la valeur du courant maximal dans la DEL DE1. Indiquer si cette valeur est compatible avec les caractéristiques de la DEL documentation technique BAN6. Justifier votre réponse.



Q13. Préciser le rôle de la structure composée de R62, R63, C57, C55. Justifier sa présence.

Q14. Déterminer la valeur moyenne de la tension sur l'entrée P0.2 du microcontrôleur.

2. Compensation

La compensation FP7 contrôle le courant dans la DEL émettrice DE1 (donc l'intensité du flux lumineux traversant le liquide à mesurer) en commandant le transistor T4 en régime linéaire à partir de la mesure du flux lumineux transmis à travers la cuve de mesure à 180° et de l'écart de la valeur mesurée par rapport à une valeur de consigne.

La mesure du flux lumineux est assurée par la photodiode de compensation puis mesurée par le convertisseur A/N (broche P0.3) du microcontrôleur.

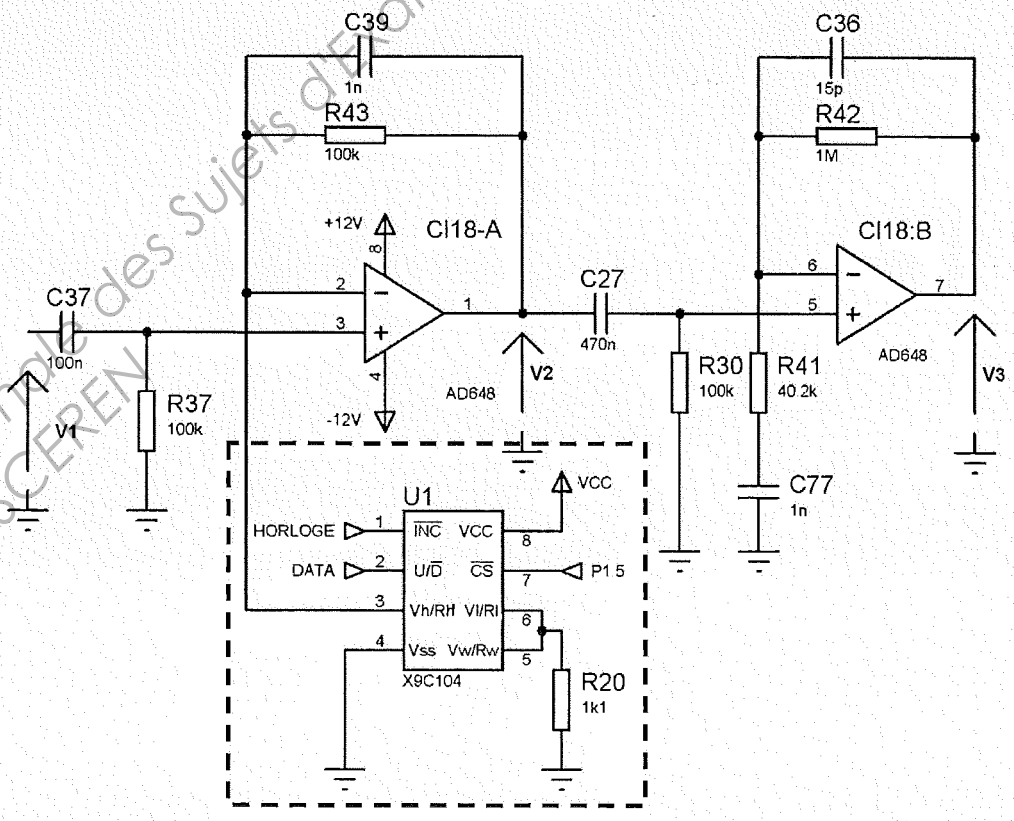
La mesure du courant moyen dans la DEL DE1 est assurée par l'entrée P0.2 du microcontrôleur.

A partir du schéma structurel BAN19

Q15. Donner la relation liant Vmesure à Vcomp en considérant que le condensateur C52 se comporte comme un circuit ouvert.

Q16. Déterminer le rôle des diodes D9 et D10.

3. Amplification à gain programmable : FS1.4



Q17. En utilisant la documentation BAN5 à BAN6, dessiner sur le document réponse BR2 le modèle équivalent du circuit en pointillé constitué de U1 et de R20 que l'on nommera Rx.

Q18. Si le compteur interne à U1 a la valeur 96, préciser alors la valeur que prend la résistance R_{u1}.

Q19. Donner l'expression de R_{u1} en fonction de la valeur N du compteur interne à U1.

Q20. Ce composant U1 étant commandé par le microcontrôleur, compléter l'algorigramme (document réponse BR3) qui permettra de faire varier sa valeur de 50kΩ à 10kΩ.

Q21. On supposera qu'à la fréquence de travail, C_{37} se comporte comme un court-circuit et C_{39} comme un circuit ouvert, établir la relation V2=f(V1).

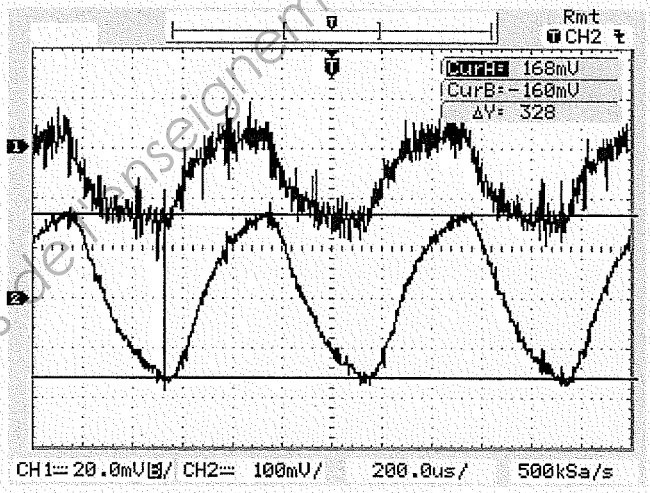
Q22. Indique le rôle de Rx.

On donne les résultats de simulation de la réponse en fréquence (document réponse BR4) de la fonction Fs1.4.

Q23. Indiquer sur le graphe à quelles valeurs de Rx correspondent les courbes minimale et maximale.

Q24. A partir des résultats de simulation, indiquer les principales caractéristiques (amplification maximale, fréquence centrale, bande passante) de la fonction FS1.4.

*Sur l'appareil en fonctionnement **(plage 0 – 10 NTU)** et pour une turbidité **T = 8 NTU**, on a relevé les chronogrammes ci-contre.*



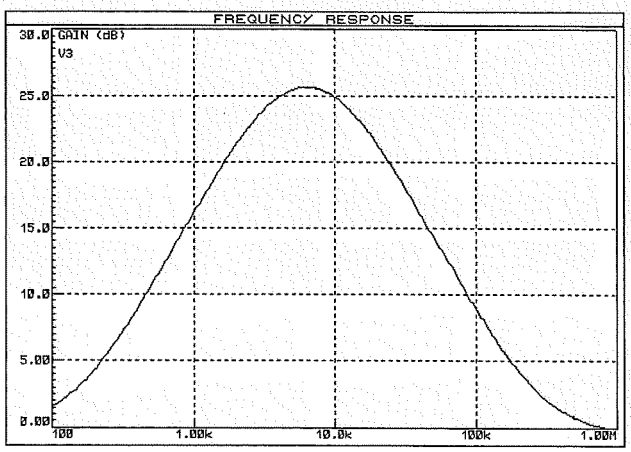
V1 (repère 1)

V2 (repère 2)

Q25. En déduire la valeur de l'amplification $A_2 = \frac{V_2}{V_1}$

Q26. Calculer la valeur de réglage de Rx correspondant à cette amplification.

Q27. A partir de la réponse en fréquence ci-contre de la fonction FS1.5 et du chronogramme donné sur le document réponse BR4, tracer sur le document réponse BR4 le chronogramme de V3=f(t) correspondant à cette valeur de réglage.



PARTIE C : Etude de la fonction FP2

Cette fonction est remplie par un microcontrôleur 16 bits de type 80C196KB (CI5) associé aux composants C8, CI2, CI3, CI4, CI6, CI10.

Schéma structurel page BAN20.

1. Mémorisation et gestion du temps

La mémorisation est assurée par plusieurs circuits :

- *la mémorisation du programme et des constantes par CI8 de référence 27C256,*
- *la mémorisation des données et des variables par CI3 de référence MK48T08,*
- *la mémorisation des données de configuration de l'appareil par CI10 de référence 93C06.*

La gestion du temps par l'horloge temps réel interne au circuit CI3 de référence MK48T08.

Q28. Compléter le document réponse BR4 dans lequel vous préciserez pour chaque mémoire, son type et sa capacité en octets.

La documentation du composant présente rapidement le bus Microwire (pages BAN8 et BAN9).

Q29. La communication de cette mémoire avec le microcontrôleur se fait avec un bus Microwire, citer deux autres types de bus utilisés pour les liaisons entres circuits intégrés.

A partir des chronogrammes donnés (document réponse BR5) répondre aux questions suivantes.

Q30. Entourer et annoter sur les chronogrammes un ***Start bit*** (***SB***), un ***Op code***, une adresse et une donnée.

Q31. Donner le rôle de la résistance R10.

Q32. On donne le contenu de la mémoire (document réponse BR5), lire sur le chronogramme concerné la valeur mémorisée puis l'entourer dans le document réponse.

Q33. On désire effacer le contenu de l'adresse 13 (valeur décimale), tracer sur le document réponse BR5 les chronogrammes correspondants.

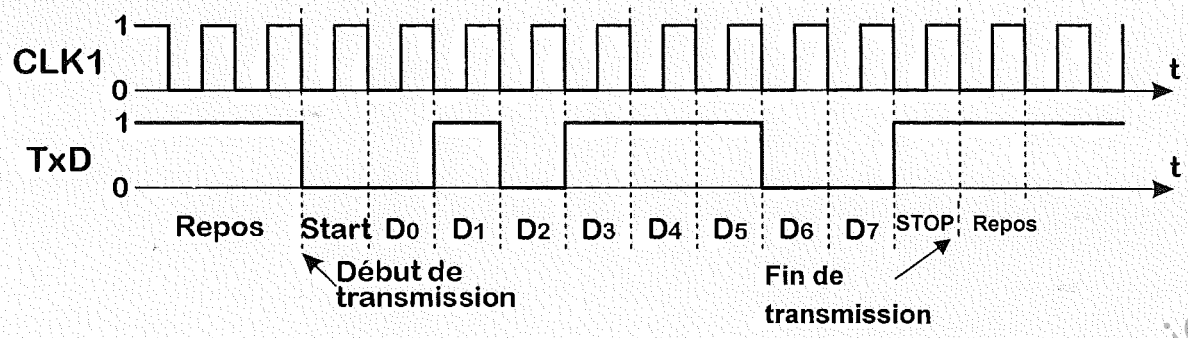
2. Etude de la fonction FP5

L'appareil peut être raccordé à un ordinateur pour le traitement des données. La liaison est de type série utilisant une boucle de courant.

Caractéristiques de la liaison :

- *vitesse : 9600bauds,*
- *1bit de start, 8bits de données, pas de parité, 1 bit de stop,*
- *au repos signal de 20mA : pas de transmission.*

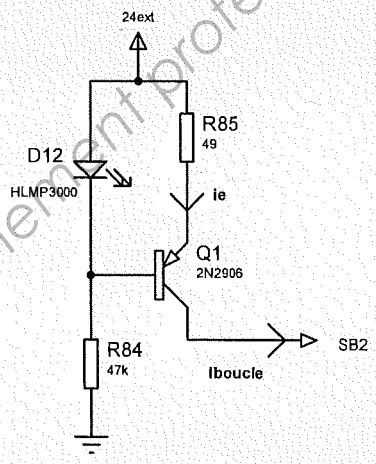
Rappel de la trame série :



Etude du générateur de courant

Caractéristiques du 2N2906 → Vce max =-40V Vbe=-0,6V Hfe= 100

HLPM3000 → Vf=1,9V à 20mA.



Q34. Etablir la relation ie=f(Vf, Vbe, R85) puis en déduire le courant Iboucle.

Q35. En vous aidant de la page12 du manuel d'utilisation BAN18, proposer une méthode simple pour tester la liaison en l'absence d'ordinateur sachant que le « turbilight » envoie régulièrement des données.

Q36. Repérer sur le chronogramme image du courant de boucle document réponse BR6, les intervalles de temps correspondants aux :

- bit de start,
- 8 bits de données,
- bit de stop.

Préciser la valeur transmise.

La vitesse de transmission est programmée à l'aide du registre BAUD_REG en vous aidant de la documentation BAN 10 à 13 :

Q37. Déterminer la valeur qu'il faut mettre dans le registre *BAUD_REG* pour obtenir la vitesse de 9600 bauds.
Compléter la fonction d'initialisation de la transmission série (document réponse BR6) pour les valeurs des registres *BAUD_REG* et *SP_CON* en mode réception.

Le circuit CI2 MB3773 (documentation technique page BAN14 à 17) contrôle la tension d'alimentation du microcontrôleur et surveille le bon déroulement du programme. En cas d'anomalie, une réinitialisation du microcontrôleur est effectuée.

Q38. Calculer le temps au bout duquel le circuit CI2 effectue un reset du microcontrôleur en cas d'anomalie logicielle.

Q39. Donner les seuils de déclenchement du reset en cas d'anomalie sur la tension d'alimentation du microcontrôleur.

Q40. Compléter le chronogramme document réponse BR7.

DOCUMENTATION

sommaire

14-stage ripple-carry binary counter/divider and oscillator

HEF4060B MSI

DESCRIPTION

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (O_3 to O_9 and O_{11} to O_{13}) and an overriding asynchronous master reset input (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (O_3 to O_9 and O_{11} to O_{13} = LOW), independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

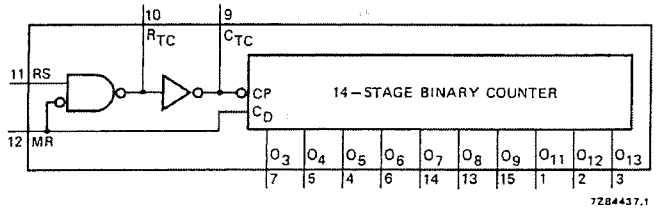


Fig.1 Functional diagram.

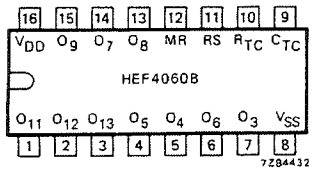


Fig.2 Pinning diagram.

PINNING

MR	master reset
RS	clock input/oscillator pin
R_{TC}	oscillator pin
C_{TC}	external capacitor connection
O_3 to O_9 O_{11} to O_{13}	counter outputs

HEF4060BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4060BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4060BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

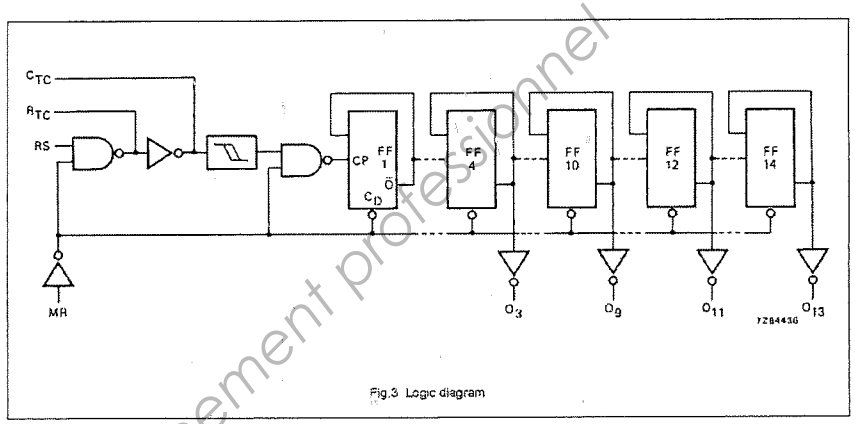


Fig.3 Logic diagram

Timing component limitations

The oscillator frequency is mainly determined by R_tC_t, provided R_t << R2 and R2C2 << R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500 Ω at V_{DD} = 5 V, 300 Ω at V_{DD} = 10 V and 200 Ω at V_{DD} = 15 V.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t \geq 100$ pF, up to any practical value,
10 kΩ ≤ R_t ≤ 1 MΩ.

Typical crystal oscillator circuit

In Fig.5, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.

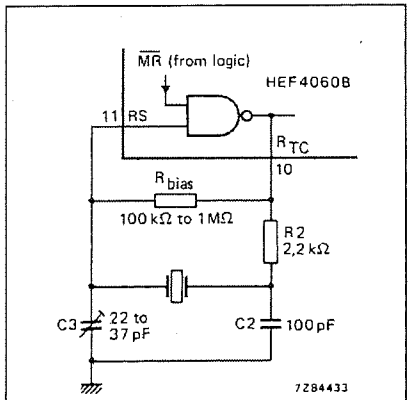


Fig.5 External component connection for crystal oscillator.

CMOS Hex Voltage Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

CD4504BT Hex Voltage Level Shifter consists of six circuits which shift input signals from the V_{CC} logic level to the V_{DD} logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the V_{CC} HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

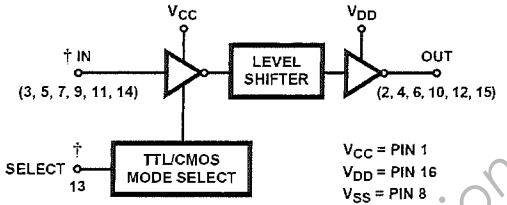
Detailed Electrical Specifications for the CD4504BT are contained in SMD 5962-96665. A "hot-link" is provided from our website for downloading.
www.intersil.com/spacedefense/newsafclasst.asp

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/quality/manuals.asp

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)
5962R9666501TEC	CD4504BDTR	-55 to 125
5962R9666501TXC	CD4504BKTR	-55 to 125

NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

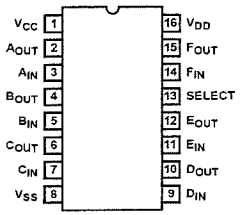


Features

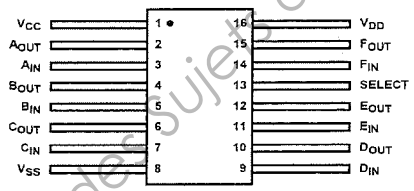
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - SEP Effective LET > 75 MEV/gm/cm^2
- Independence of Power Supply Sequence Considerations
  - V_{CC} Can Exceed V_{DD}
  - Input Signals can Exceed Both V_{CC} and V_{DD}
- Up and Down Level Shifting Capability
- Shiftable Input Threshold for Either CMOS or TTL Compatibility
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics

Pinouts

CD4504BT (SBDIP), CDIP2-T16
TOP VIEW



CD4504BT (FLATPACK), CDFP4-16
TOP VIEW



Schottky barrier diodes — BYV10 series

FEATURES

- Low switching losses
- Fast recovery time
- Guard ring protected
- Hermetically sealed leaded glass package.

APPLICATIONS

- Low power, switched-mode power supplies
- Rectifying
- Polarity protection.

DESCRIPTION

The BYV10-20 to BYV10-40 types are Schottky barrier diodes fabricated in planar technology, and encapsulated in SOD81 hermetically sealed glass packages incorporating Implotec™(1) technology.

(1) Implotec is a trademark of Philips.

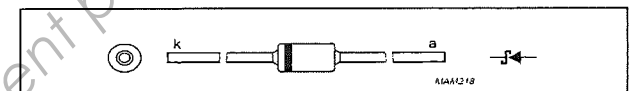


Fig.1 Simplified outline (SOD81) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage				
	BYV10-20		–	20	V
	BYV10-30		–	30	V
	BYV10-40		–	40	V
$I_{F(AV)}$	average forward current	note 1	–	1	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	125	°C

Note

1. Refer to SOD81 standard mounting conditions.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_F	forward voltage	I_F = 0.1 A	–	–	390	mV
		I_F = 1 A	–	–	550	mV
		I_F = 3 A	–	–	850	mV
I_R	reverse current	$V_R = V_{RRMmax}$; note 1	–	–	1	mA
C_d	diode capacitance	V_R = 0 V; f = 1 MHz	–	220	–	pF

Note

1. Pulsed test: t_p = 300 µs; δ = 0.02.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	100	K/W

Note

1. Refer to SOD81 standard mounting conditions.

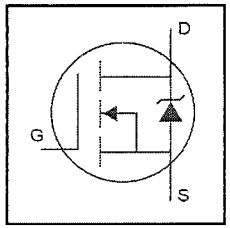
International
IOR Rectifier

PD - 9.1672A

IRFZ34E

HEXFET® Power MOSFET

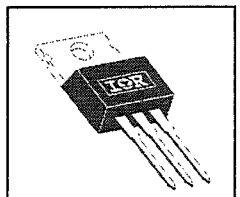
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling



V_{DSS} = 60V

$R_{DS(on)}$ = 0.042Ω

I_D = 28A



Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	28	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	20	
I_{DM}	Pulsed Drain Current ①	112	
P_D @T_C = 25°C	Power Dissipation	68	W
	Linear Derating Factor	0.46	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	97	mJ
I_{AR}	Avalanche Current①	17	A
E_{AR}	Repetitive Avalanche Energy①	6.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	2.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	——	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	——	62	

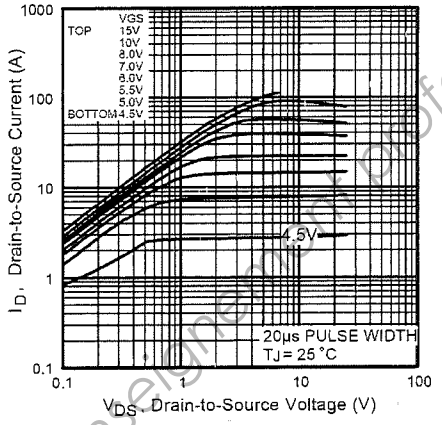


Fig 1. Typical Output Characteristics

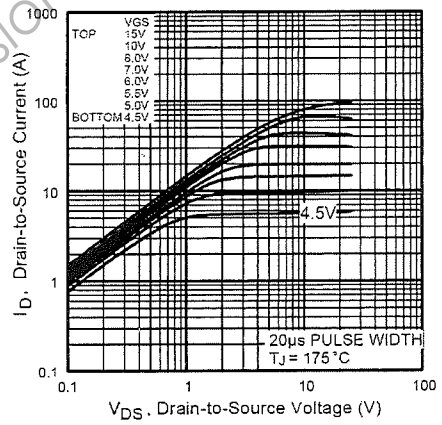


Fig 2. Typical Output Characteristics

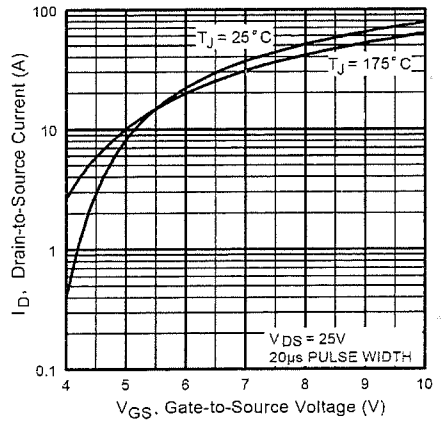


Fig 3. Typical Transfer Characteristics

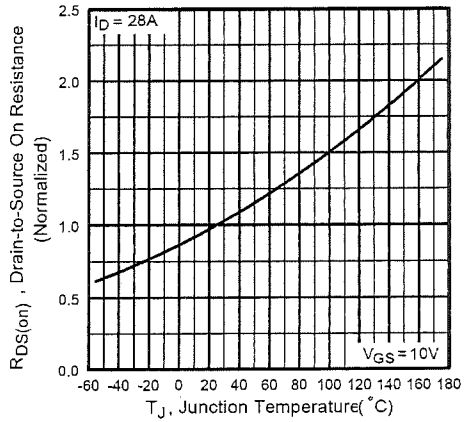


Fig 4. Normalized On-Resistance Vs. Temperature

Digitally Controlled Potentiometer (XDCP™)

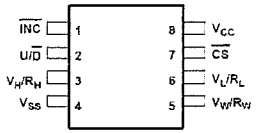
The X9C102, X9C103, X9C104, X9C503 are Intersils' digitally controlled (XDCP) potentiometers. The device consists of a resistor array, wiper switches, a control section, and non-volatile memory. The wiper position is controlled by a three-wire interface.

The potentiometer is implemented by a resistor array composed of 99 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in non-volatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications ranging from control to signal processing to parameter adjustment.

Pinout

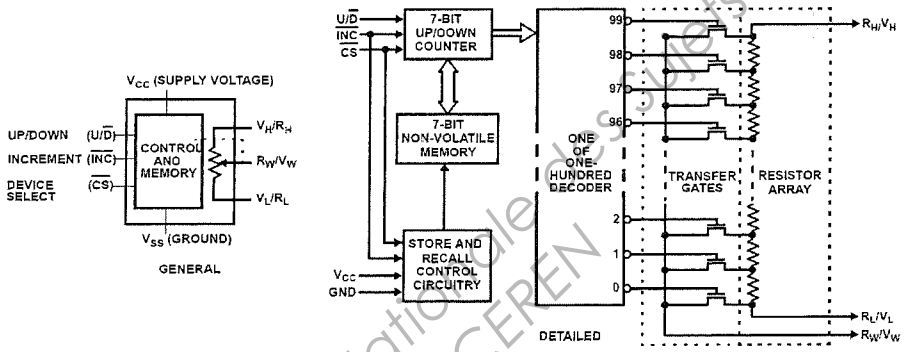
X9C102, X9C103, X9C104, X9C503
(8 LD SOIC, 8 LD PDIP)
TOP VIEW



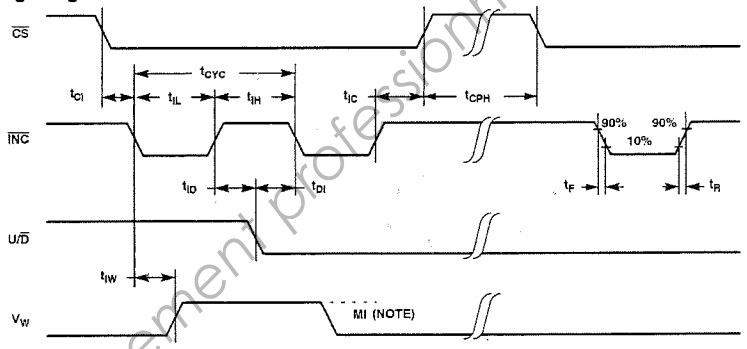
Features

- Solid-State Potentiometer
- Three-Wire Serial Interface
- 100 Wiper Tap Points
  - Wiper Position Stored in Non-volatile Memory and Recalled on Power-up
- 99 Resistive Elements
  - Temperature Compensated
  - End-to-End Resistance, ±20%
  - Terminal Voltages, ±5V
- Low Power CMOS
  - V_{CC} = 5V
  - Active Current, 3mA max.
  - Standby Current, 750µA max.
- High Reliability
  - Endurance, 100,000 Data Changes per Bit
  - Register Data Retention, 100 years
- X9C102 = 1kΩ
- X9C103 = 10kΩ
- X9C503 = 50kΩ
- X9C104 = 100kΩ
- Packages
  - 8 Ld SOIC
  - 8 Ld PDIP
- Pb-Free Available (RoHS Compliant)

Block Diagram



AC Timing Diagram



NOTE: MI REFERS TO THE MINIMUM INCREMENTAL CHANGE IN THE V_W OUTPUT DUE TO A CHANGE IN THE WIPER POSITION.

Pin Descriptions

R_H/V_H and R_L/V_L

The high (V_H/R_H) and low (V_L/R_L) terminals of the ISLX9C102, X9C103, X9C104, X9C503 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is -5V and the maximum is +5V. The terminology of V_H/R_H and V_L/R_L references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W/V_W

V_W/R_W is the wiper terminal, and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in non-volatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the ISLX9C102, X9C103, X9C104, X9C503 device will be placed in the low power standby mode until the device is selected once again.

Principles of Operation

There are three sections of the X9C102, X9C103, ISL9C104 and ISL9C503: the input control, counter and decode section; the non-volatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions, the contents of the counter can be stored in non-volatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a "make-before-break" mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W/R_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the non-volatile memory. When power is restored, the contents of the memory are recalled and the wiper is reset to the value last stored.

The internal charge pump allows a wide range of voltages (from -5V to 5V) applied to XDCP terminals yet given a convenience of single power supply. The typical charge pump noise of 20mV at 850kHz should be taken in consideration when designing an application circuit.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a 7-bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The value of the counter is stored in non-volatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9Cxxx, move the wiper and deselect the device without having to store the latest wiper position in non-volatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-down/up cycle recalled the previously stored data.

This procedure allows the system to always power-up to a pre-set value stored in non-volatile memory; then during system operation, minor adjustments could be made. The adjustments might be based on user preference, i.e.: system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then

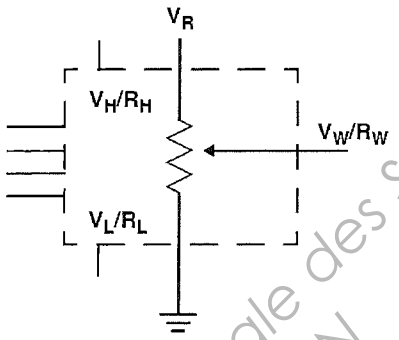
Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper Up
L	↘	L	Wiper Down
↗	H	X	Store Wiper Position
H	X	X	Standby Current
↗	L	X	No Store, Return to Standby
↘	L	H	Wiper Up (not recommended)
↘	L	L	Wiper Down (not recommended)

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
——	Must be steady	Will be steady
⫽	May change from Low to High	Will change from Low to High
⫽	May change from High to Low	Will change from High to Low
⋈	Don't Care: Changes Allowed	Changing: State Not Known
⋈	N/A	Center Line is High Impedance

Basic Configurations of Electronic Potentiometers



STANLEY

Package 3-3J1

DNK5306X

Through-hole IRED/
φ5 High Speed, High Total Output Power Type

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Absolute Maximum Ratings	Unit
Power Dissipation	Pd	170	mW
Forward Current	I_F	100	mA
Pulse Forward Current ※1	I_{FRM}	1,000	mA
Derating (Ta=25℃ or higher)	ΔI_F	1.33	mA/℃
	ΔI_{FRM}	13.3	mA/℃
Reverse Voltage	V_R	5	V
Operating Temperature	T_{opr}	-30~+85	℃
Storage Temperature	T_{stg}	-30~+100	℃

※1 I_{FRM} Measurement condition : Pulse Width≦ 0.1ms, Duty≦ 1/100

Item	Conditions	Symbol	Characteristics		Unit
Forward Voltage	I_F=50mA	V_F	MIN.	1.3	V
			TYP.	1.5	
			MAX.	1.7	
Reverse Current	V_R=5V	I_R	MAX.	100	μA
Radiant Intensity	I_F=50mA	I_E	MIN.	33.6	mW/sr
			TYP.	75	
Total Output Power	I_F=50mA	Po	TYP.	24	mW
Peak Wavelength	I_F=50mA	λ_p	TYP.	870	nm
Spectral Half-width	I_F=50mA	$\Delta\lambda$	TYP.	45	nm
Half Intensity Angle	I_F=50mA	2θ 1/2	TYP.	20	deg.
Cut-off Frequency	I_F=50mA$_{DC}$±5mA, -3db from 1MHz	fc	MIN.	(40)	MHz
			TYP.	55	
Response Time	I_F=50mA	tr/tf	TYP.	7/7	ns
Pulse Forward Voltage	I_{FRM}=500mA	V_{FM}	Max.	3.4	V

MICROCHIP

27C256

256K (32K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 90 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - 28-pin Thin Small Outline Package (TSOP)
  - 28-pin Very Small Outline Package (VSOP)
  - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

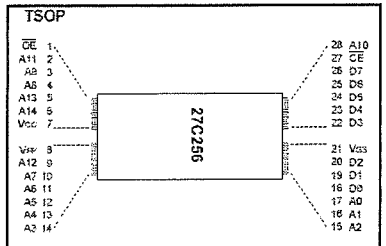
DESCRIPTION

The Microchip Technology Inc. 27C256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

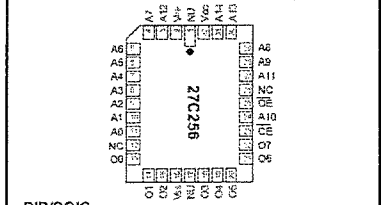
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, VSOP or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

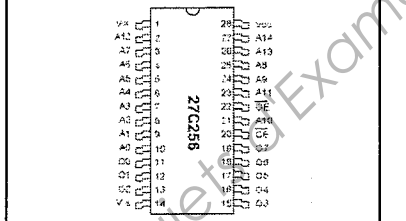
TSOP



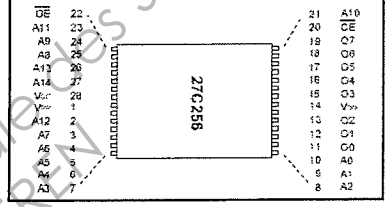
PLCC



DIP/SOIC



VSOP

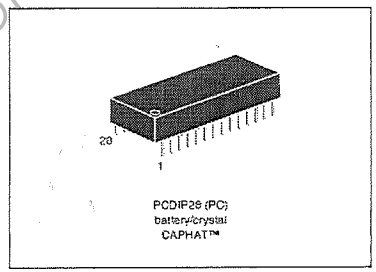


M48T08
M48T08Y, M48T18

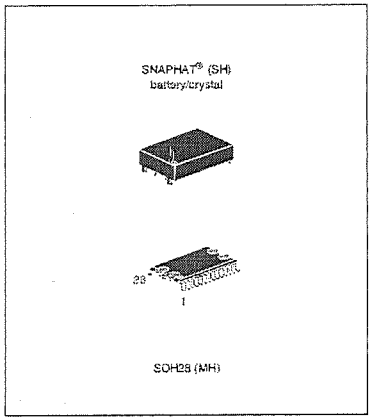
5 V, 64 Kbit (8 Kb x 8) TIMEKEEPER® SRAM

Features

- Integrated ultra low power SRAM, real-time clock, power-fail control circuit, and battery
- BYTEWIDE™ RAM-like clock access
- BCD coded year, month, day, date, hours, minutes, and seconds
- Typical clock accuracy of ±1 minute a month, at 25 °C
- Automatic power-fail chip deselect and write protection
- Write protect
  V_{PFD} = Power-fail deselect voltage):
  - M48T08: V_{CC} = 4.75 to 5.5 V
    4.5 V ≤ V_{PFD} ≤ 4.75 V
  - M48T18/T08Y: V_{CC} = 4.5 to 5.5 V
    4.2 V ≤ V_{PFD} ≤ 4.5 V
- Software controlled clock calibration for high accuracy applications
- Self-contained battery and crystal in the CAPHAT™ DIP package
- Packaging includes a 28-lead SOIC and SNAPHAT® top (to be ordered separately)
- SOIC package provides direct connection for a snaphat top which contains the battery and crystal
- Pin and function compatible with DS1643 and JEDEC standard 8 K x 8 SRAMs
- RoHS compliant
  - Lead-free second level interconnect



PCDIP28 (PC)
battery/crystal
CAPHAT™



SOH28 (MH)

National Semiconductor

August 1996

NM93C06/C46/C56/C66 256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

NM93C06/C46/C56/C66 256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE Bus Interface)

General Description

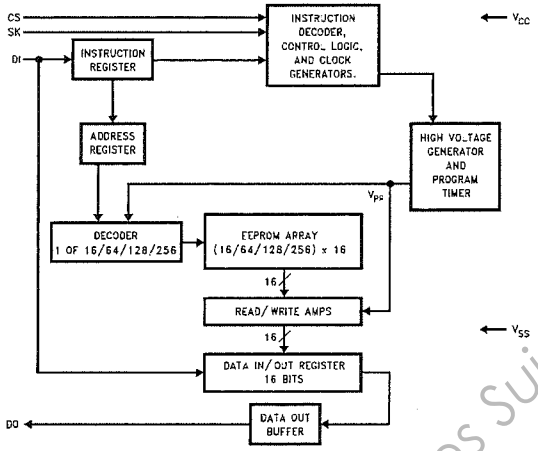
The NM93C06/C46/C56/C66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in both SO and TSSOP packages for small space considerations.

The EEPROM Interfacing is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- Device status during programming mode
- Typical active current of 200 μA; Typical standby current of 10 μA
- No erase required before write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

Block Diagram

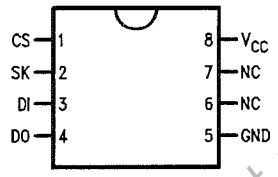


TL/D/10751–1

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
MICROWIRE™ is a trademark of National Semiconductor Corporation.

Connection Diagrams

Dual-In-Line Package (N)
8-Pin SO (M8) and 8-Pin TSSOP (MT8)



TL/D/10751–2

Top View

See NS Package Number
N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06–NM93C66	0°C to +70°C
NM93C06E–NM93C66E	−40°C to +85°C
NM93C06V–NM93C66V	−40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ± 10% unless otherwise specified

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current	NM93C06-NM93C66 NM93C06E/V-NM93C66E/V	CS = V_{IH}, SK = 1 MHz SK = 1 MHz		1 1	mA
I_{CCS}	Standby Current	NM93C06-NM93C66 NM93C06E/V-NM93C66E/V	CS = V_{IL}		50 50	μA μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 3)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93C06-NM93C66 NM93C06E/V-NM93C66E/V	(Note 4)	0 0	1 1	MHz
t_{SKH}	SK High Time	NM93C06-NM93C66 NM93C06E/V-NM93C66E/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time	NM93C06-NM93C66 NM93C06E/V-NM93C66E/V	(Note 2)	250 250		ns

Functional Description

The NM93C06/C46/C56/C66 devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

All Data in signals are clocked into the device on the low-to-high SK transition.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the selected register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

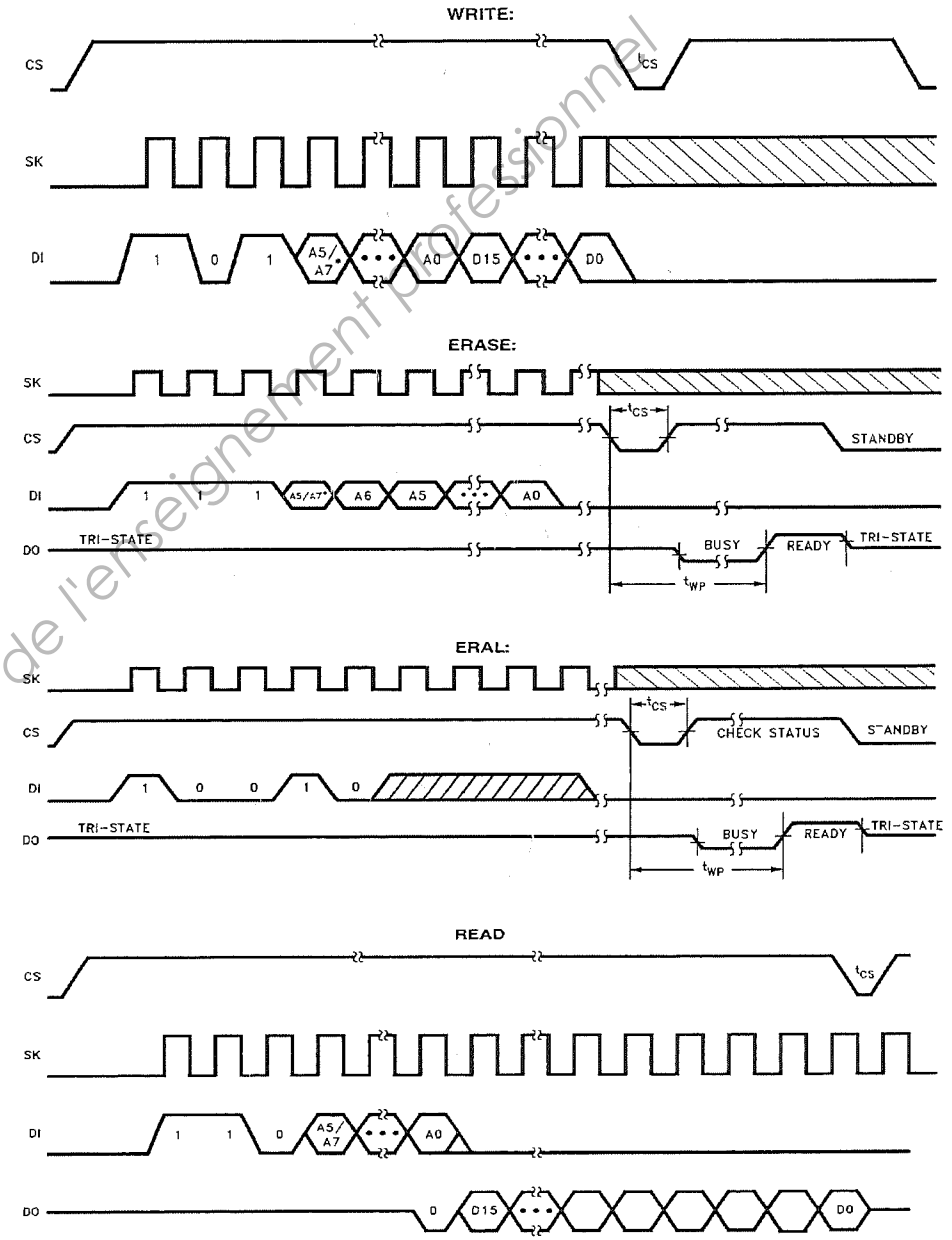
To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

NOTE: The NSC CMOS EEPROMs do not require an 'ERASE' or 'ERASE ALL' operation prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06 and NM93C46

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, at specified address.
WEN	1	00	11XXXX		Enable all programming modes.
ERASE	1	11	A5–A0		Erase selected register.
WRITE	1	01	A5–A0	D15–D0	Writes selected register.
ERAL	1	00	10XXXX		Erases all registers.
WRALL	1	00	01XXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXX		Disables all programming modes.

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06.



10.0 SERIAL PORT

The serial port on the 80C196KB has one synchronous and 3 asynchronous modes. The asynchronous modes

are full duplex, meaning they can transmit and receive at the same time. The receiver is double buffered so that the reception of a second byte can begin before the first byte has been read. The transmitter on the 80C196KB is also double buffered allowing continuous transmissions. The port is functionally compatible with the serial port on the MCS-51 family of microcontrollers, although the software controlling the ports is different.

Data to and from the serial port is transferred through SBUF(RX) and SBUF(TX), both located at 07H. SBUF(TX) holds data ready for transmission and SBUF(RX) contains data received by the serial port. SBUF(TX) and SBUF(RX) can be read and can be written in Window 15.

Mode 0, the synchronous shift register mode, is designed to expand I/O over a serial line. Mode 1 is the standard 8 bit data asynchronous mode used for normal serial communications. Modes 2 and 3 are 9 bit data asynchronous modes typically used for interprocessor communications. Mode 2 provides monitoring of a communication line for a 1 in the 9th bit position before causing an interrupt. Mode 3 causes interrupts independant of the 9th bit value.

10.1 Serial Port Status and Control

Control of the serial port is done through the Serial Port Control (SP__CON) register shown in Figure 10-1. Writing to location 11H accesses SP__CON while reading it accesses SP__STAT. The upper 3 bits of SP__CON must be written as 0s for future compatibility. On the 80C196KB the SP__STAT register contains new bits to indicate receive Overrun Error (OE), Framing Error (FE), and Transmitter Empty (TXE). The bits which were also present on the 8096BH are the Transmit Interrupt (TI) bit, the Receive Interrupt (RI) bit, and the Received Bit 8 (RB8) or Receive Parity Error (RPE) bit. SP__STAT is read-only in Window 0 and is shown in Figure 10-1.

In all modes, the RI flag is set after the last data bit is sampled, approximately in the middle of a bit time. Data is held in the receive shift register until the last data bit is received, then the data byte is loaded into SBUF (RX). The receiver on the 80C196KB also checks for a valid stop bit. If a stop bit is not found within the appropriate time, the Framing Error (FE) bit is set.

Since the receiver is double-buffered, reception on a second data byte can begin before the first byte is read. However, if data in the shift register is loaded into SBUF (RX) before the previous byte is read, the Overflow Error (OE) bit is set. Regardless, the data in SBUF (RX) will always be the latest byte received; it will never be a combination of the two bytes. The RI, FE, and OE flags are cleared when SP__STAT is read. However, RI does not have to be cleared for the serial port to receive data.

SP__CON:	7	6	5	4	3	2	1	0	
	X	X	X	TB8	REN	PEN	M2	M1	11H

TB8 — Sets the ninth data bit for transmission. Cleared after each transmission. Not valid if parity is enabled.

REN — Enables the receiver

PEN — Enables the Parity function (even parity)

M2, M1 — Sets the mode. Mode0 = 00, Mode1 = 01, Mode2 = 10, Mode3 = 11

SP__STAT	7	6	5	4	3	2	1	0	
	RB8/ RPE	RI	TI	FE	TXE	OE	X	X	11H

RB8 — Set if the 9th data bit is high on reception (parity disabled)

RPE — Set if parity is enabled and a parity error occurred

RI — Set after the last data bit is sampled

TI — Set at the beginning of the STOP bit transmission

FE — Set if no STOP bit is found at the end of a reception

TXE — Set if two bytes can be transmitted

OE — Set if the receiver buffer is overwritten

Figure 10-1. Serial Port Control and Status Registers

The Transmitter Empty (TXE) bit is set if the transmit buffer is empty and ready to take up to two characters. TXE gets cleared as soon as a byte is written to SBUF. Two bytes may be written consecutively to SBUF if TXE is set. One byte may be written if TI alone is set. By definition, if TXE has just been set, a transmission has completed and TI will be set. The TI bit is reset when the CPU reads the SP__STAT registers.

The TB8 bit is cleared after each transmission and both TI and RI are cleared when SP__STAT read. The RI and TI status bits can be set by writing to SP__STAT in window 15 but they will not cause an interrupt. Reading of SP__CON in Window 15 will read the last value written. Whenever the TXD pin is used for the serial port it must be enabled by setting IOC1.5 to a 1. I/O control register 1 can be read in window 15 to determine the setting.

STARTING TRANSMISSIONS AND RECEPTIONS

In Mode 0, if REN = 0, writing to SBUF (TX) will start a transmission. Causing a rising edge on REN, or clearing RI with REN = 1, will start a reception. Setting REN = 0 will stop a reception in progress and inhibit further receptions. To avoid a partial or complete undesired reception, REN must be set to zero before RI is cleared. This can be handled in an interrupt environment by using software flags or in straight-line code by using the Interrupt Pending register to signal the completion of a reception.

In the asynchronous modes, writing to SBUF (TX) starts a transmission. A falling edge on RXD will begin a reception if REN is set to 1. New data placed in SBUF (TX) is held and will not be transmitted until the end of the stop bit has been sent.

In all modes, the RI flag is set after the last data bit is sampled approximately in the middle of the bit time. Also for all modes, the TI flag is set after the last data bit (either 8^{th} or 9^{th}) is sent, also in the middle of the bit time. The flags clear when SP__STAT is read, but do not have to be clear for the port to receive or transmit. The serial port interrupt bit is set as a logical OR of the RI and TI bits. Note that changing modes will reset the Serial Port and abort any transmission or reception in progress on the channel.

BAUD RATES

Baud rates are generated based on either the T2CLK pin or XTAL1 pin. The values used are different than those used for the 8096BH because the 80C196KB uses a divide-by-2 clock instead of a divide-by-3 clock to generate the internal timings. Baud rates are calculated using the following formulas where BAUD__REG is the value loaded into the baud rate register:

Asynchronous Modes 1, 2 and 3:

$$\text{BAUD\_\_REG} = \frac{\text{XTAL1}}{\text{Baud Rate} * 16} - 1 \text{ OR } \frac{\text{T2CLK}}{\text{Baud Rate} * 8}$$

Synchronous Mode 0:

$$\text{BAUD\_\_REG} = \frac{\text{XTAL1}}{\text{Baud Rate} * 2} - 1 \text{ OR } \frac{\text{T2CLK}}{\text{Baud Rate}}$$

The most significant bit in the baud register value is set to a one to select XTAL1 as the source. If it is a zero the T2CLK pin becomes the source. The following table shows some typical baud rate values.

BAUD RATES AND BAUD REGISTER VALUES

Baud Rate	XTAL1 Frequency		
	8.0 MHz	10.0 MHz	12.0 MHz
300	1666 / −0.02	2082 / 0.02	2499 / 0.00
1200	416 / −0.08	520 / −0.03	624 / 0.00
2400	207 / 0.16	259 / 0.16	312 / −0.16
4800	103 / 0.16	129 / 0.16	155 / 0.16
9600	51 / 0.16	64 / 0.16	77 / 0.16
19.2K	25 / 0.16	32 / 1.40	38 / 0.16

Baud Register Value / % Error

A maximum baud rate of 750 Kbaud is available in the asynchronous modes with 12 MHz on XTAL1. The synchronous mode has a maximum rate of 3.0 Mbaud with a 12 MHz clock. Location 0EH is the Baud Register. It is loaded sequentially in two bytes, with the low byte being loaded first. This register may not be loaded with zero in serial port Mode 0.

10.2 Serial Port Interrupts

The serial port generates one of three possible interrupts: Transmit Interrupt TI(2030H), Receive Interrupt RI(2032H) and SERIAL(200CH). When the RI bit gets set an interrupt is generated through either 200CH or 2032H depending on which interrupt is enabled. INT__MASK1.1 controls the serial port receive interrupt through location 2032H and INT__MASK.6 controls serial port interrupts through location 200CH. The 8096BH shared the TI and RI interrupts on the SERIAL interrupt vector. On the 80C196KB, these interrupts share both the serial interrupt vector and have their own interrupt vectors.

When the TI bit is set it can cause an interrupt through the vectors at locations 200CH or 2030. Interrupt through location 2030 is determined by INT__MASK1.0. Interrupts through the serial interrupt is controlled by the same bit as the RI interrupt(INT__MASK.6). The user should not mask off the serial port interrupt when using the double-buffered feature of the transmitter, as it could cause a missed count in the number of bytes being transmitted.

10.3 Serial Port Modes

MODE 0

Mode 0 is a synchronous mode which is commonly used for shift register based I/O expansion. In this

mode the TXD pin outputs a set of 8 pulses while the RXD pin either transmits or receives data. Data is transferred 8 bits at a time with the LSB first. A diagram of the relative timing of these signals is shown in Figure 10-2. Note that this is the only mode which uses RXD as an output.

Mode 0 Timings

In Mode 0, the TXD pin sends out a clock train, while the RXD pin transmits or receives the data. Figure 10-2 shows the waveforms and timing.

In this mode the serial port expands the I/O capability of the 80C196KB by simply adding shift registers. A schematic of a typical circuit is shown in Figure 10-3. This circuit inverts the data coming in, so it must be reinverted in software.

MODE 1

Mode 1 is the standard asynchronous communications mode. The data frame used in this mode is shown in Figure 10-4. It consists of 10 bits; a start bit (0), 8 data bits (LSB first), and a stop bit (1). If parity is enabled by setting SPCON.2, an even parity bit is sent instead of the 8th data bit and parity is checked on reception.

MODE 2

Mode 2 is the asynchronous 9th bit recognition mode. This mode is commonly used with Mode 3 for multiprocessor communications. Figure 10-4 shows the data frame used in this mode. It consists of a start bit (0), 9 data bits (LSB first), and a stop bit (1). When transmitting, the 9th bit can be set to a one by setting the TB8 bit in the control register before writing to SBUF (TX). The TB8 bit is cleared on every transmission, so it must be set prior to writing to SBUF (TX). During reception, the serial port interrupt and the Receive Interrupt will not occur unless the 9th bit being received is set. This provides an easy way to have selective reception on a data link. Parity cannot be enabled in this mode.

MODE 3

Mode 3 is the asynchronous 9th bit mode. The data frame for this mode is identical to that of Mode 2. The transmission differences between Mode 3 and Mode 2 are that parity can be enabled (PEN = 1) and cause the 9th data bit to take the even parity value. The TB8 bit can still be used if parity is not enabled (PEN = 0). When in Mode 3, a reception always causes an interrupt, regardless of the state of the 9th bit. The 9th bit is stored if PEN = 0 and can be read in bit RB8. If PEN = 1 then RB8 becomes the Receive Parity Error (RPE) flag.

ASSP

Power Supply Monitor with Watch-Dog Timer

MB3773

■ DESCRIPTION

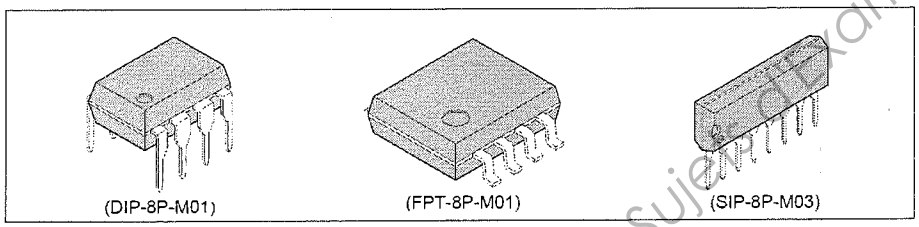
MB3773 generates the reset signal to protect an arbitrary system when the power-supply voltage momentarily is intercepted or decreased. It is IC for the power-supply voltage watch and "Power on reset" is generated at the normal return of the power supply. MB3773 sends the microprocessor the reset signal when decreasing more than the voltage, which the power supply of the system specified, and the computer data is protected from an accidental deletion.

In addition, the watchdog timer for the operation diagnosis of the system is built into, and various microprocessor systems can provide the fail-safe function. If MB3773 does not receive the clock pulse from the processor for an specified period, MB3773 generates the reset signal.

■ FEATURES

- Precision voltage detection (V_S = 4.2 V ± 2.5 %)
- Detection threshold voltage has hysteresis function
- Low voltage output for reset signal (V_{CC} = 0.8 V Typ)
- Precision reference voltage output (V_R = 1.245 V ± 1.5%)
- With built-in watchdog timer of edge trigger input.
- External parts are few.(1 piece in capacity)
- The reset signal outputs the positive and negative both theories reason.

■ PACKAGES

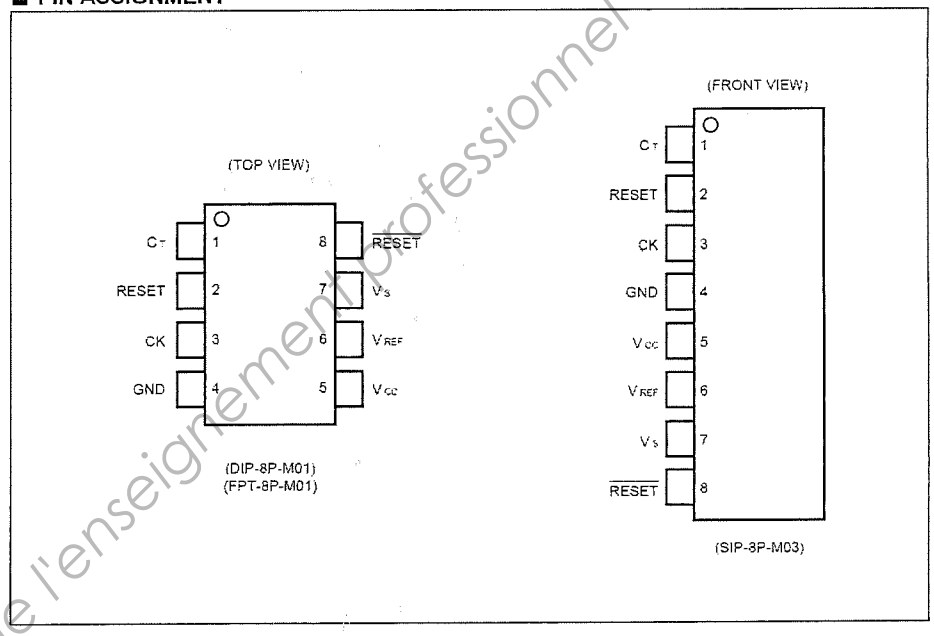


(DIP-8P-M01) (FPT-8P-M01) (SIP-8P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit

FUJITSU

■ PIN ASSIGNMENT

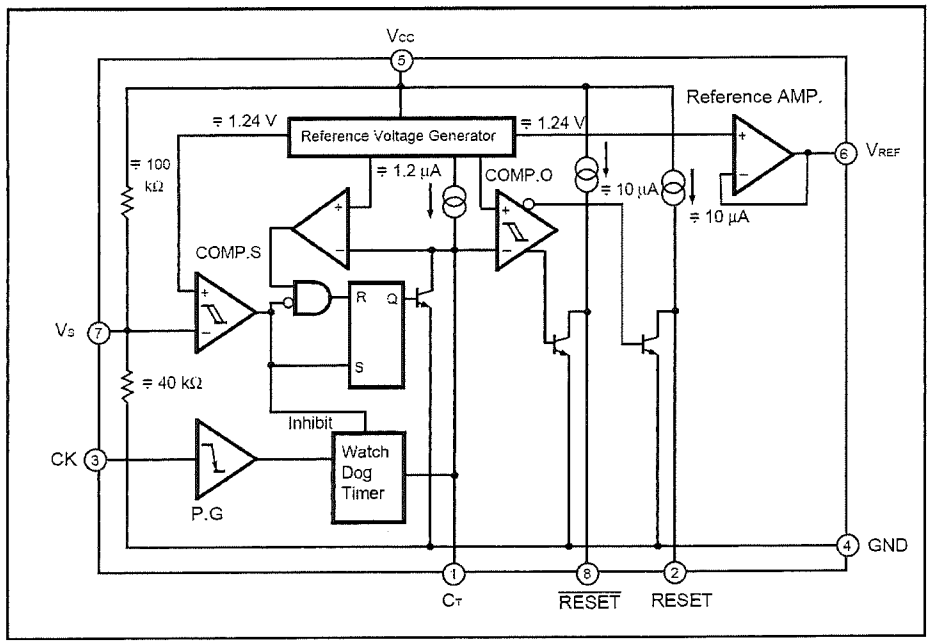


■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply voltage	V_{CC}	− 0.3	+ 18	V
Input voltage	V_S	− 0.3	V_{CC} + 0.3 (≤ +18)	V
	V_{CK}	− 0.3	+ 18	V
$\overline{RESET}$, RESET Supply voltage	V_{OH}	− 0.3	V_{CC} + 0.3 (≤ +18)	V
Power dissipation (Ta ≤ +85 °C)	P_D	—	200	mW
Storage temperature	T_{STG}	− 55	+ 125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

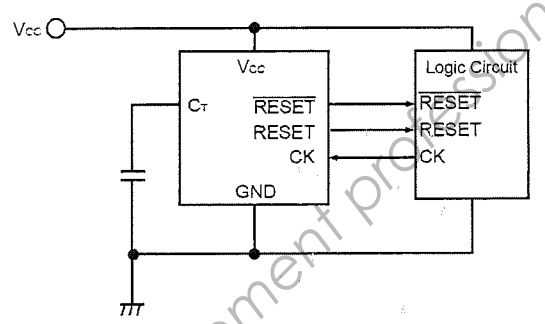
■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTIONS

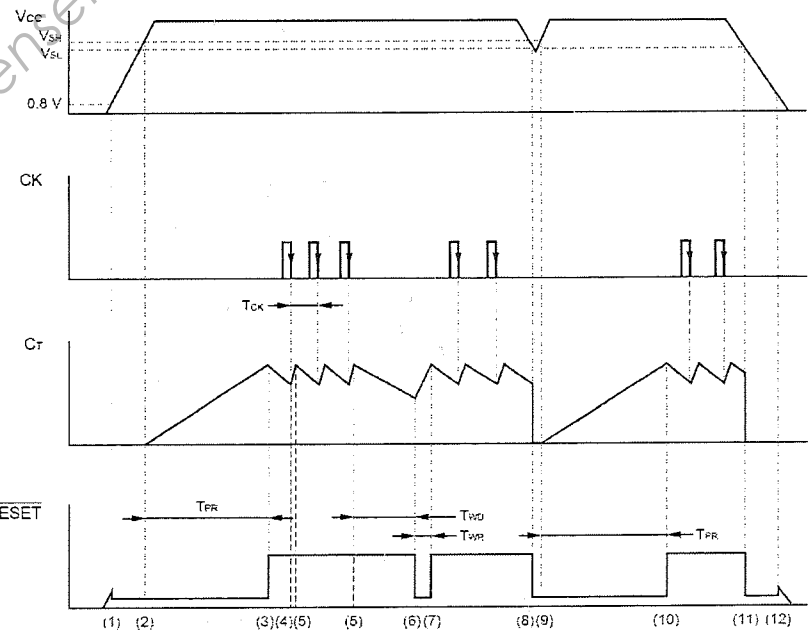
Comp.S is comparator including hysteresis. it compare the reference voltage and the voltage of Vs, so that when the voltage of Vs terminal falls below approximately 1.23 V, reset signal outputs.
Instantaneous breaks or drops in the power can be detected as abnormal conditions by the MB3773 within a 2 µs interval.
However because momentary breaks or drops of this duration do not cause problems in actual systems in some cases, a delayed trigger function can be created by connecting capacitors to the Vs terminal.
Comp.O is comparator for turning on/off the output and, compare the voltage of the Cr terminal and the threshold voltage. Because the RESET/$\overline{\text{RESET}}$ outputs have built-in pull-up circuit, there is no need to connect to external pull-up resistor when connected to a high impedance load such as CMOS logic IC.
(It corresponds to 500 kΩ at Vcc = 5 V.) when the voltage of the CK terminal changes from the "high" level into the "Low" level, pulse generator is sent to the watch-dog timer by generating the pulse momentarily at the time of drop from the threshold level.
When power-supply voltages fall more than detecting voltages, the watch-dog timer becomes a interdiction.
The Reference amplifier is a op-amp to output the reference voltage.
If the comparator is put up outside, two or more power-supply voltage monitor and overvoltage monitor can be done.
If it uses a comparator of the open-collector output, and the output of the comparator is connected with the Vs terminal of MB3773 without the pull-up resistor, it is possible to voltage monitor with reset-hold time.

• **MB3773 Basic Operation**



T_{PR} (ms) ∓ 1000 · C_T (µF)
T_{WD} (ms) ∓ 100 · C_T (µF)
T_{WR} (ms) ∓ 20 · C_T (µF)

Example ; C_T = 0.1 µF
T_{RR} (ms) ∓ 100 (ms)
T_{WD} (ms) ∓ 10 (ms)
T_{WR} (ms) ∓ 2 (ms)



■ OPERATION SEQUENCE

(1) When Vcc rises to about 0.8 V, $\overline{\text{RESET}}$ goes "Low" and RESET goes "High".
The pull-up current of approximately 1 μA (Vcc = 0.8 V) is output from RESET.

(2) When Vcc rises to V_{SH} (≒ 4.3V) , the charge with C_T starts.
At this time, the output is being reset.

(3) When C_T begins charging, $\overline{\text{RESET}}$ goes "High" and RESET goes "Low".
After T_{PR} reset of the output is released.
Reset hold time: T_{PR} (ms) ≒ 1000 × C_T (μF)
After releasing reset, the discharge of C_T starts, and watch-dog timer operation starts.
T_{PR} is not influenced by the CK input.

(4) C changes from the discharge into the charge if the clock (Negative edge) is input to the CK terminal while discharging C_T.

(5) C changes from the charge into the discharge when the voltage of C_T reaches a constant threshold (≒ 1.4 V) .
(4) and (5) are repeated while a normal clock is input by the logic system.

(6) When the clock is cut off, gets, and the voltage of C_T falls on threshold (≒ 0.4 V) of reset on. $\overline{\text{RESET}}$ goes "Low" and RESET goes "High".
Discharge time of C_T until reset is output: T_{WD} is watch-dog timer monitoring time.
T_{WD} (ms) ≒ 100 × C_T (μF)
Because the charging time of C_T is added at accurate time from stop of the clock and getting to the output of reset of the clock, T_{WD} becomes maximum $T_{WD} + T_{WR}$ by minimum T_{WD}.

(7) Reset time in operating watch-dog timer:T_{WR} is charging time where the voltage of C_T goes up to off threshold (≒ 1.4 V) for reset.
T_{WR} (ms) ≒ 20 × C_T (μF)
Reset of the output is released after C_T reaches an off threshold for reset, and C_T starts the discharge, after that if the clock is normally input, operation repeats (4) and (5) , when the clock is cut off, operation repeats (6) and (7) .

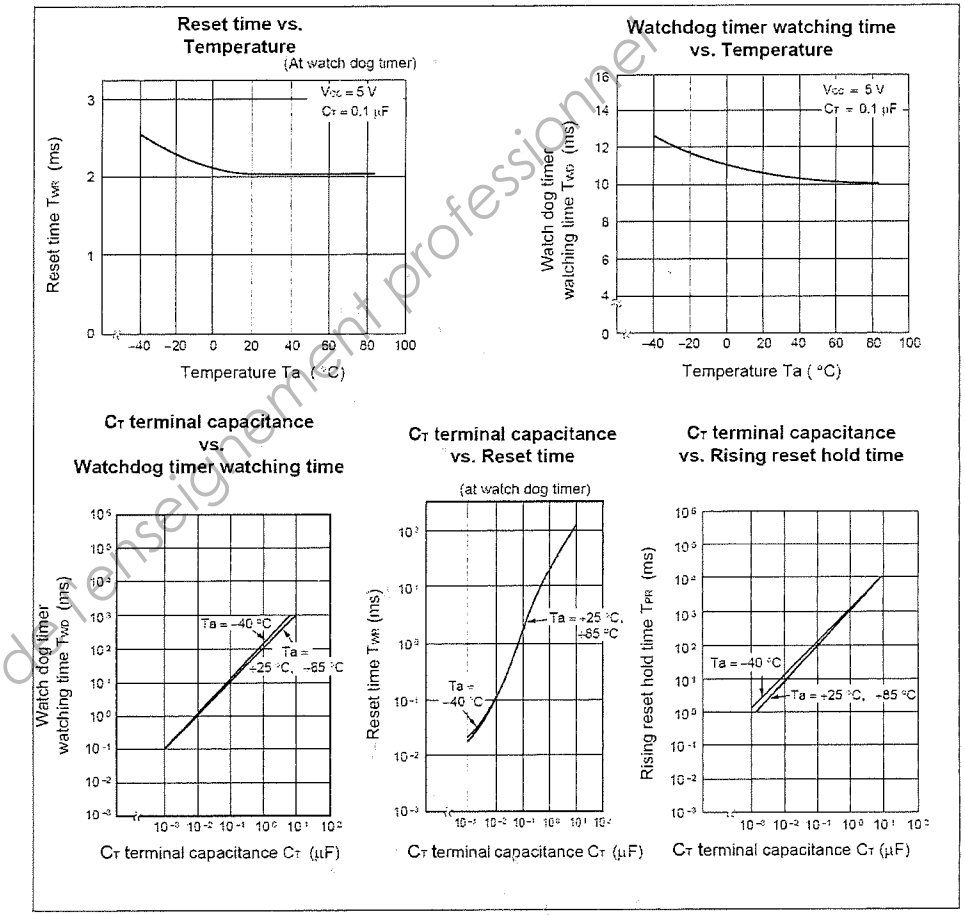
(8) When Vcc falls on V_{SL} (≒ 4.2 V) , reset is output. C_T is rapidly discharged of at the same time.

(9) When Vcc goes up to V_{SH}, the charge with C_T is started.
When Vcc is momentarily low,
After falling V_{SL} or less Vcc, the time to going up is the standard value of the Vcc input pulse width in V_{SH} or more.
After the charge of C_T is discharged, the charge is started if it is T_{PI} or more.

(10) Reset of the output is released after T_{PR}, after Vcc becomes V_{SH} or more, and the watch-dog timer starts.
After that, when Vcc becomes V_{SL} or less, (8) to (10) is repeated.

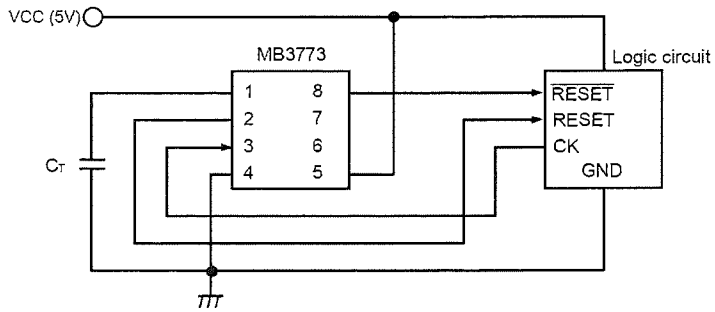
(11) While power supply is off, when Vcc becomes V_{SL} or less, reset is output.

(12) The reset output is maintained until Vcc becomes 0.8 V when Vcc falls on 0 V.



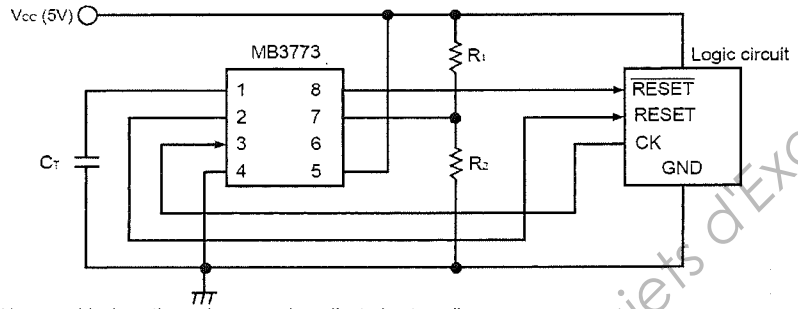
■ APPLICATION CIRCUIT

EXAMPLE 1: Monitoring 5V Supply Voltage and Watchdog Timer



Notes : • Supply voltage is monitored using V_S.
• Detection voltage are V_{SH} and V_{SL}.

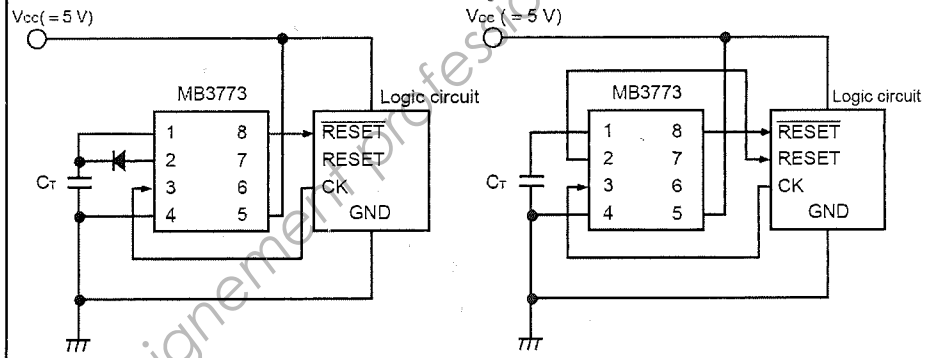
EXAMPLE 2: 5V Supply Voltage Monitoring (external fine-tuning type)



Notes : • Vs detection voltage can be adjusted externally.
• Based on selecting R_1 and R_2 values that are sufficiently lower than the resistance of the IC's internal voltage divider, the detection voltage can be set according to the resistance ratio of R_1 and R_2 (See the table below.)

R_1 (kΩ)	R_2 (kΩ)	Detection voltage: V_{SL} (V)	Detection voltage: V_{SH} (V)
10	3.9	4.4	4.5
9.1	3.9	4.1	4.2

EXAMPLE 9: Reducing Reset Hold Time

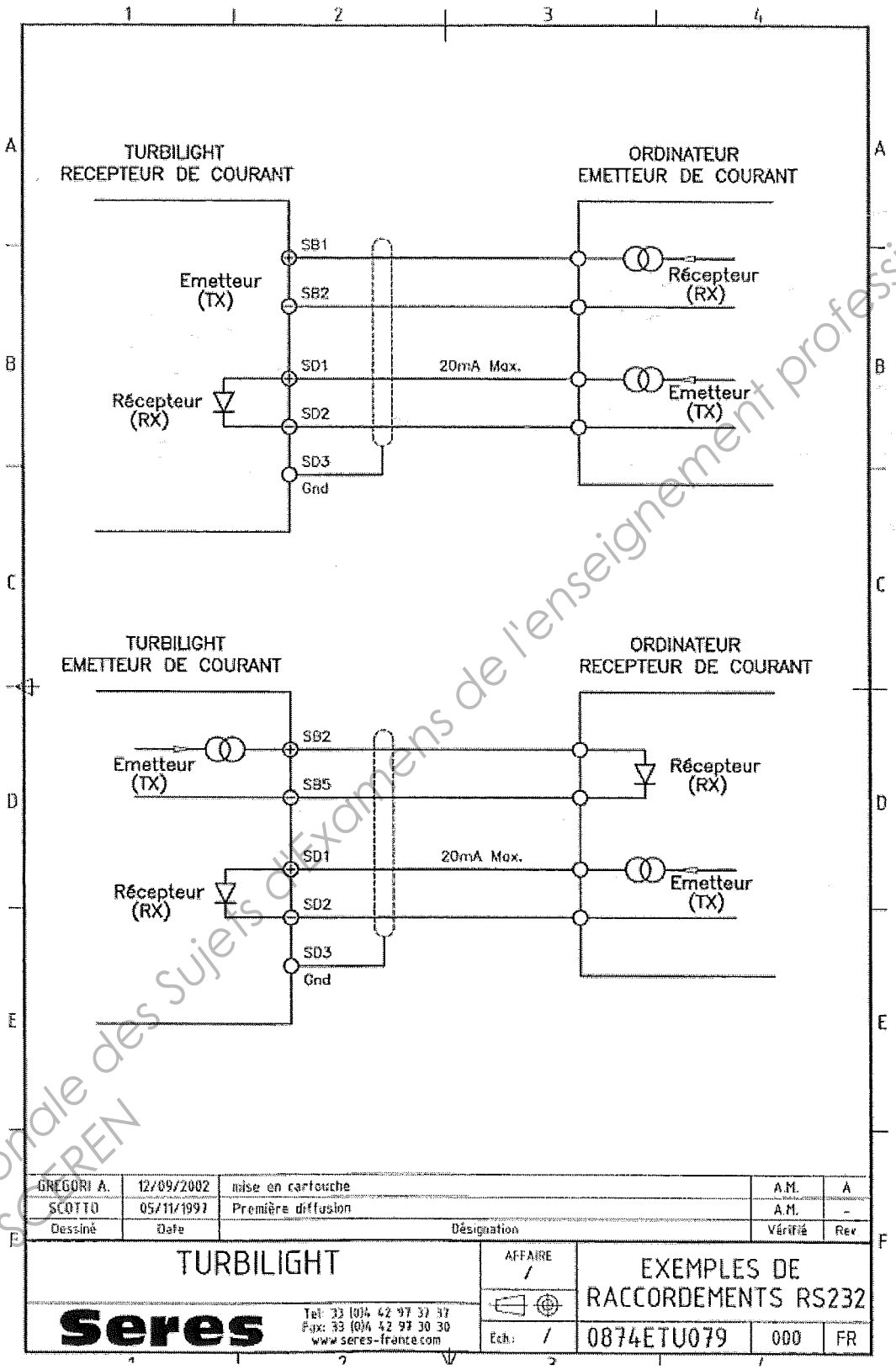


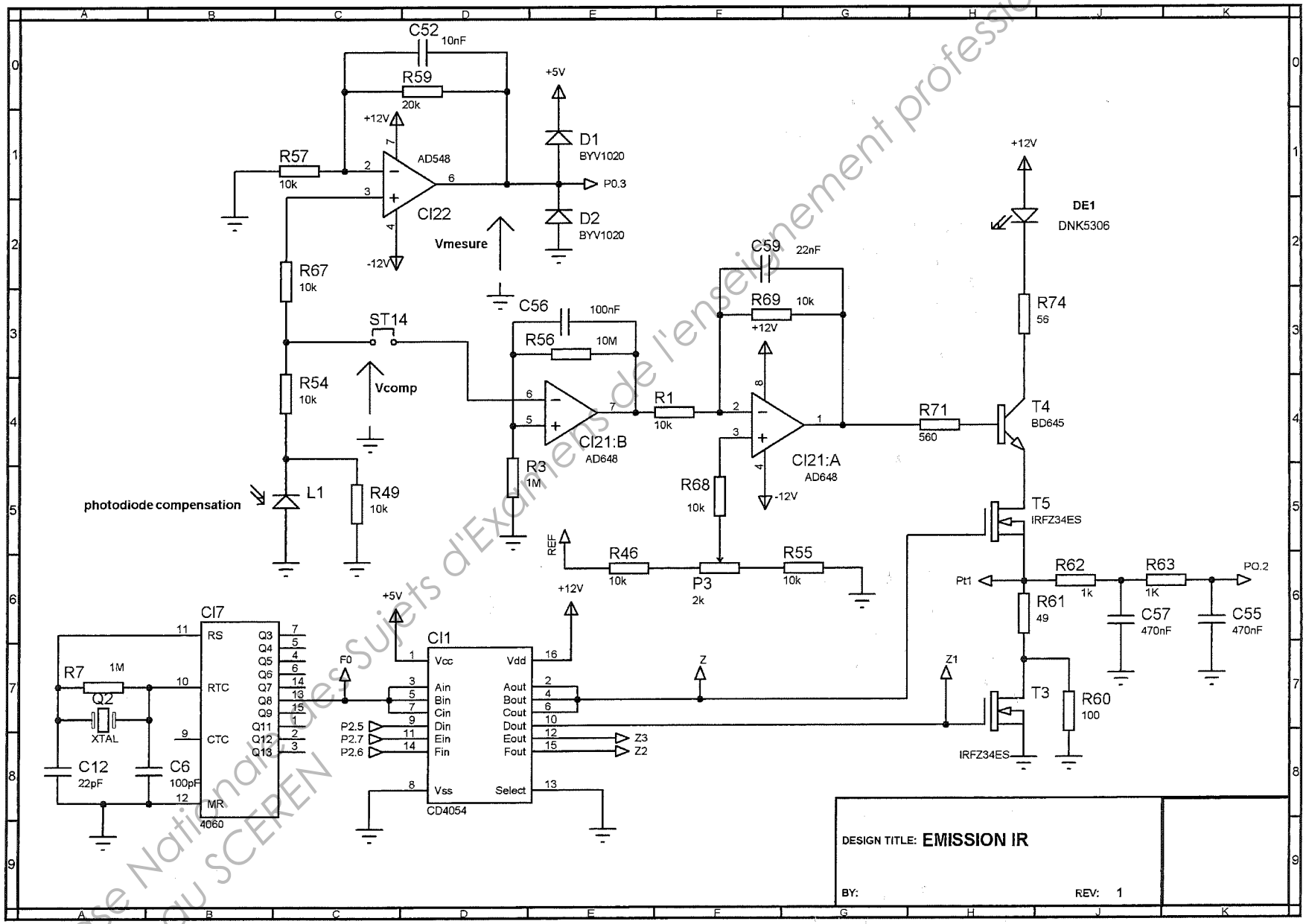
(a) T_{PR} reduction method (b) Standard usage

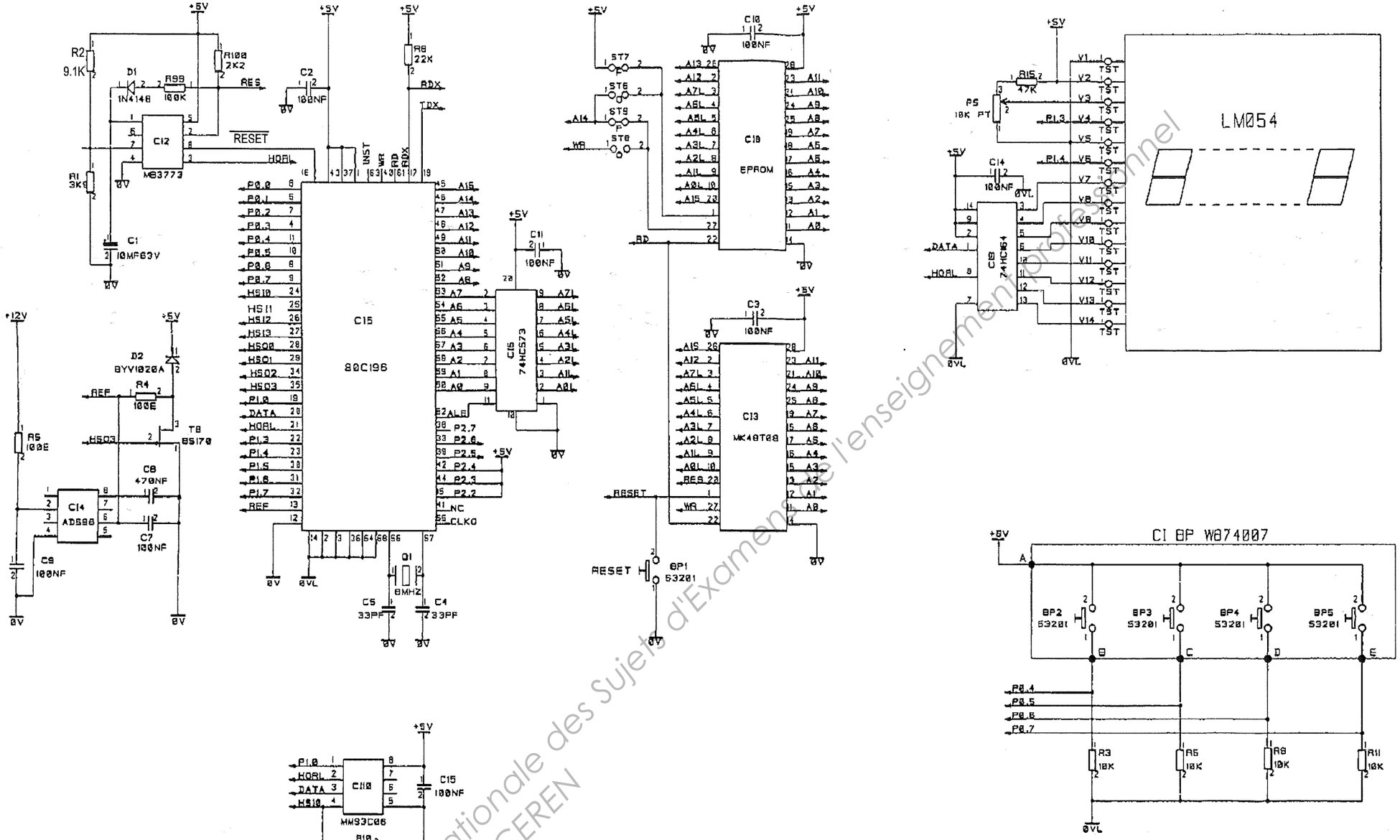
Notes : • $\overline{\text{RESET}}$ is the only output that can be used.
• Standard T_{PR}, T_{WD} and T_{WR} value can be found using the following formulas.
Formulas: T_{PR} (ms) ≒ 100 × C_T (μF)
T_{WD} (ms) ≒ 100 × C_T (μF)
T_{WR} (ms) ≒ 16 × C_T (μF)
• The above formulas become standard values in determining T_{PR}, T_{WD} and T_{WR}.
Reset hold time is compared below between the reduction circuit and the standard circuit.

C_T = 0.1 μF

	T_{PR} reduction circuit	Standard circuit
T_{PR} ≒	10 ms	100 ms
T_{WD} ≒	10 ms	10 ms
T_{WR} ≒	1.6 ms	2.0 ms







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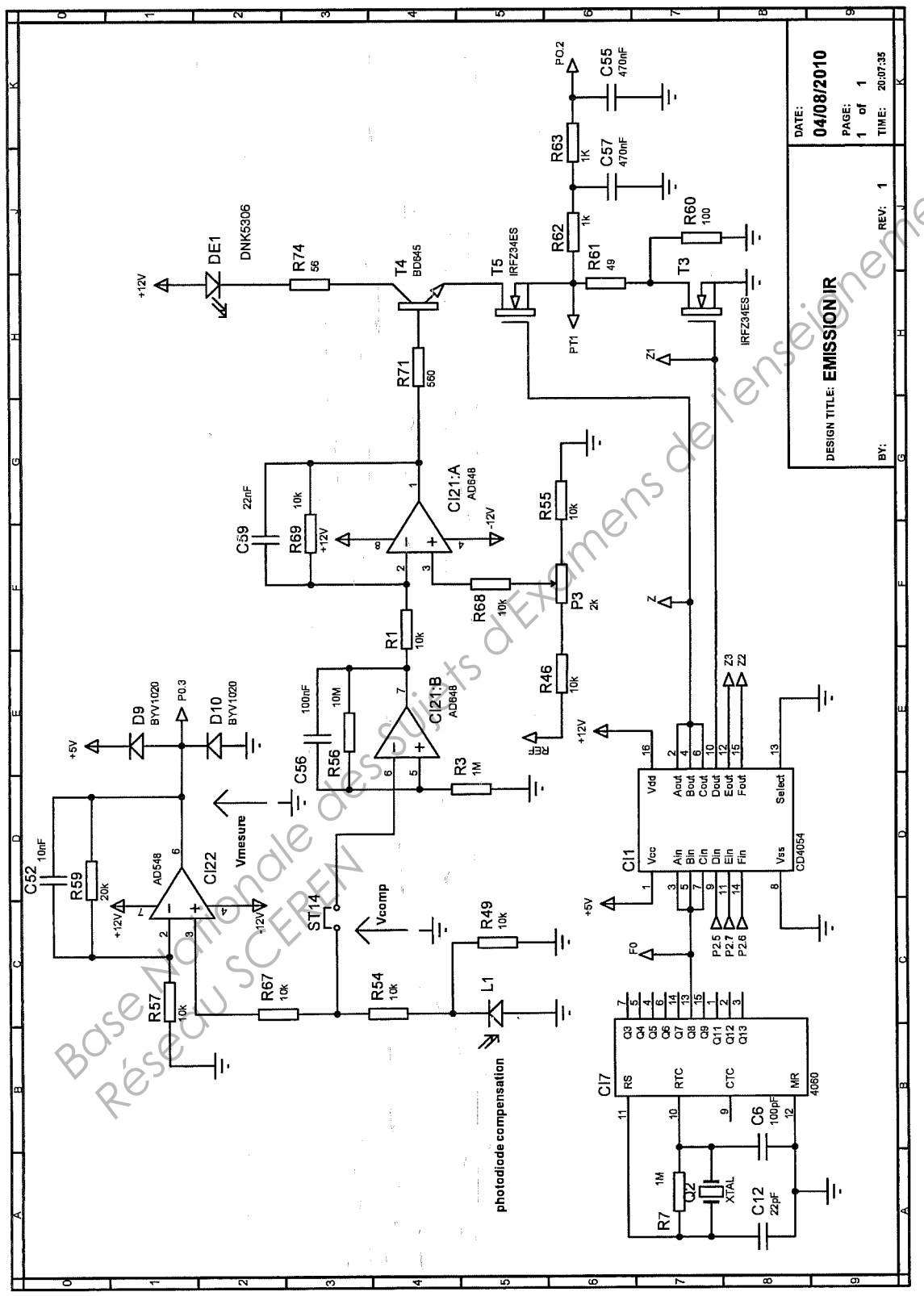
DOCUMENTS RÉPONSE

Q8.



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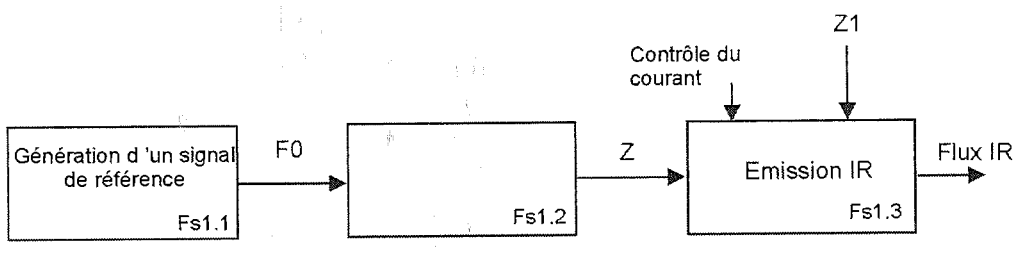
Q9.



Q10. Q11.

Abréviations : (B)=Bloqué ; (P)=Passant ; (A)= Allumée ; (E) =Éteinte ;

Z1	Z	État de T3	État de T5	Modèle équivalent T3	Modèle équivalent T5	État de la DEL IR DE1
0V	0V					
0V	+12V					
+12V	0V					
+12V	+12V					

Q17. Modèle équivalent

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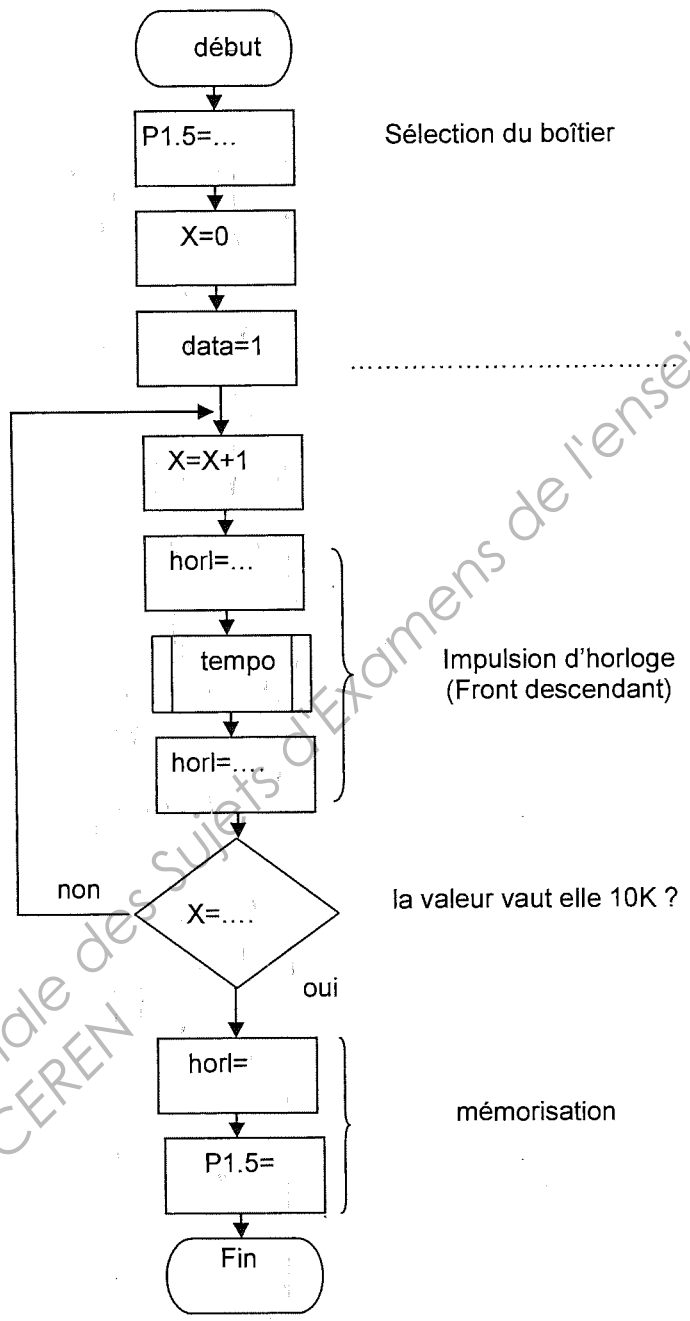
Q20.

Remarque le sigle "horl" représente Horloge



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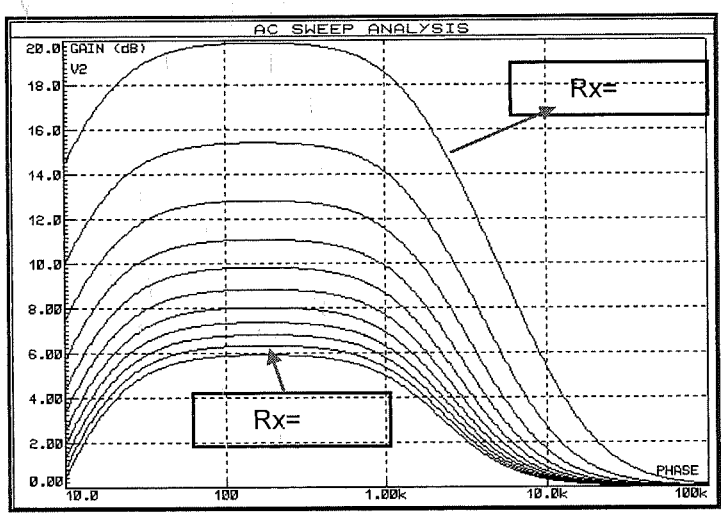
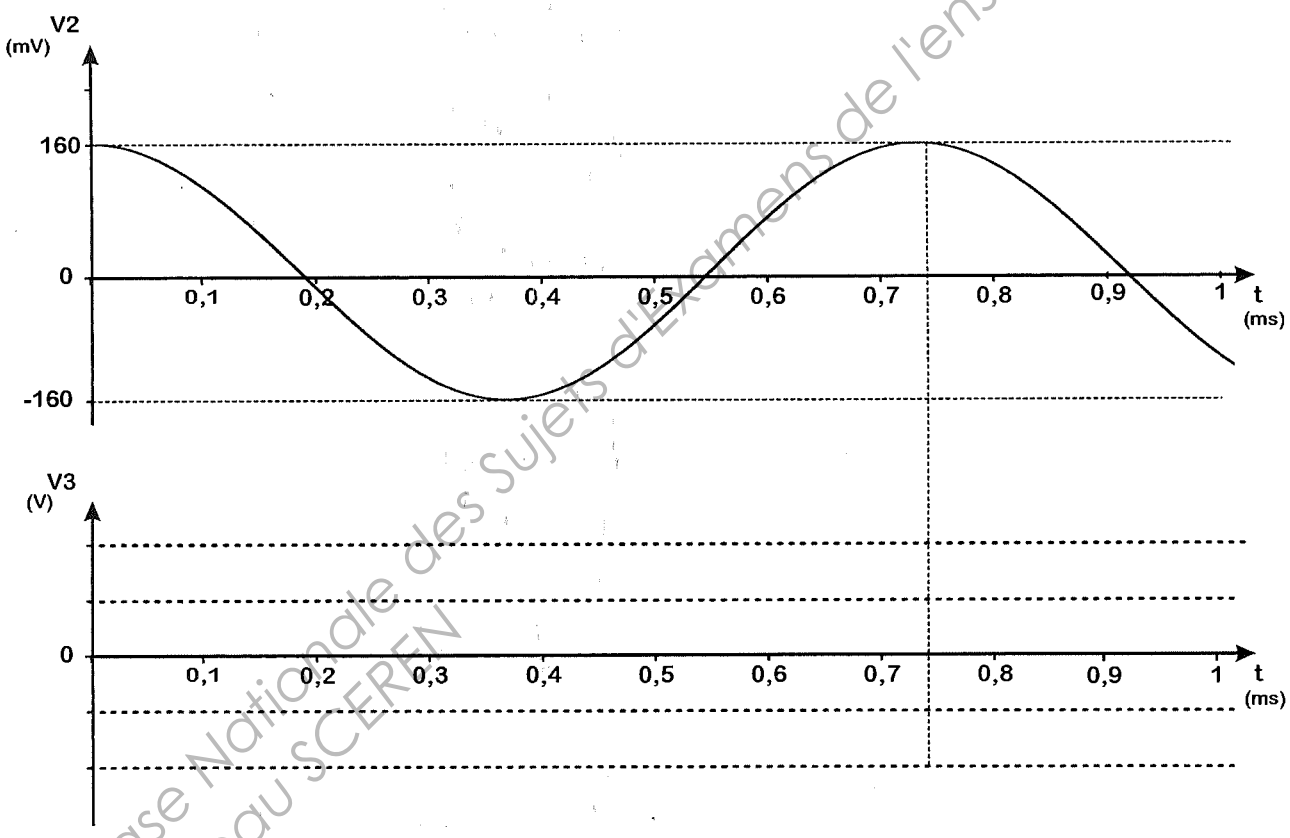
Q23.



Q27.



Q28.

Repère schéma	Référence	Type	Capacité en octets
CI8	27C256		
CI3	MK48T08		
CI10	93C06		

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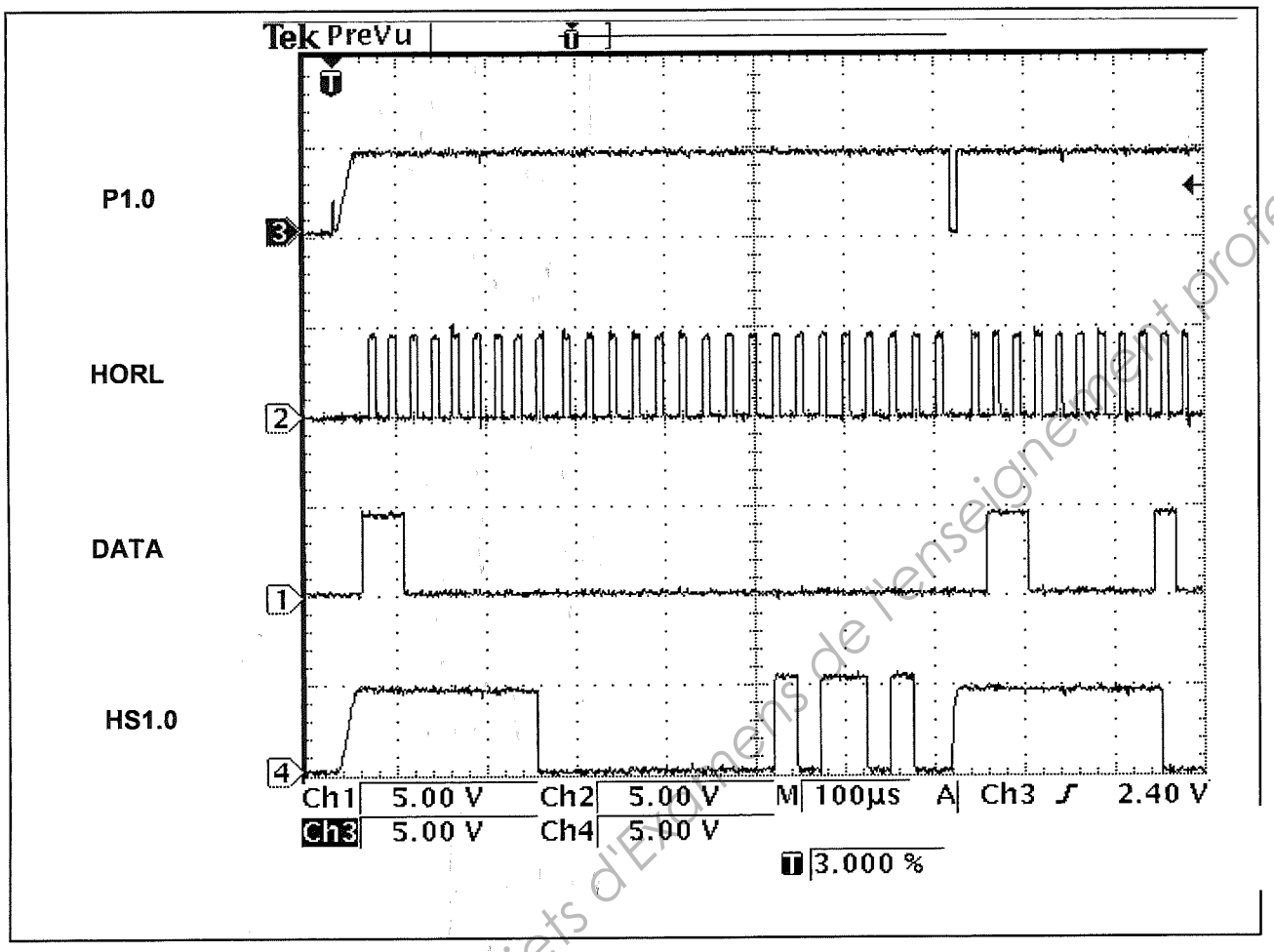
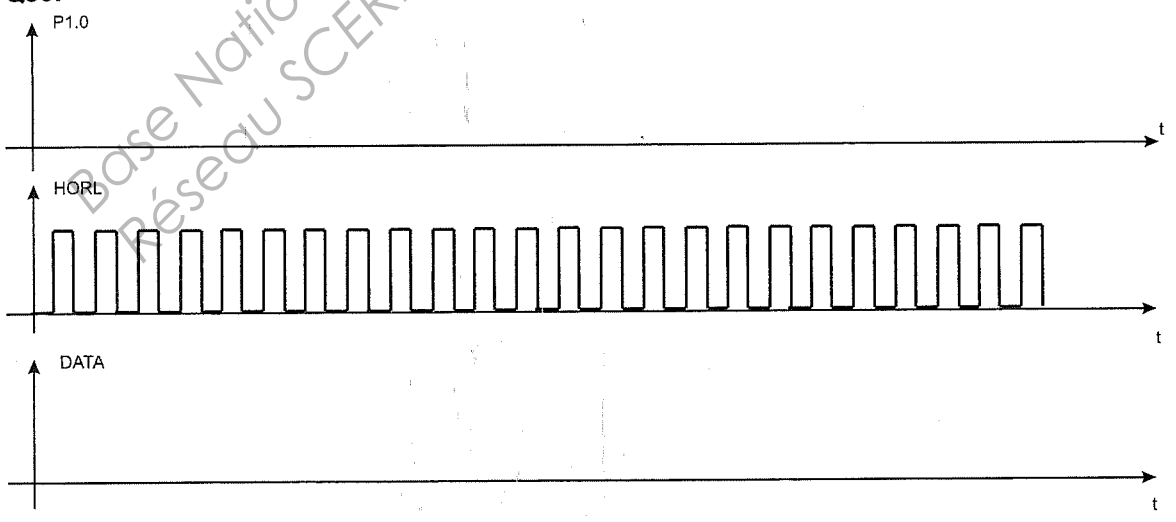
Q30.



Q32.

```
00000  5A 00 C8 06 D8 01 FA 00 --8A 02 06 00 1E 00 3C 00 Z.............<.
00010  01 00 DC 05 04 02 20 03 --64 00 E8 03 0A 00 64 00 ...... .d.....d.
```

Q33.



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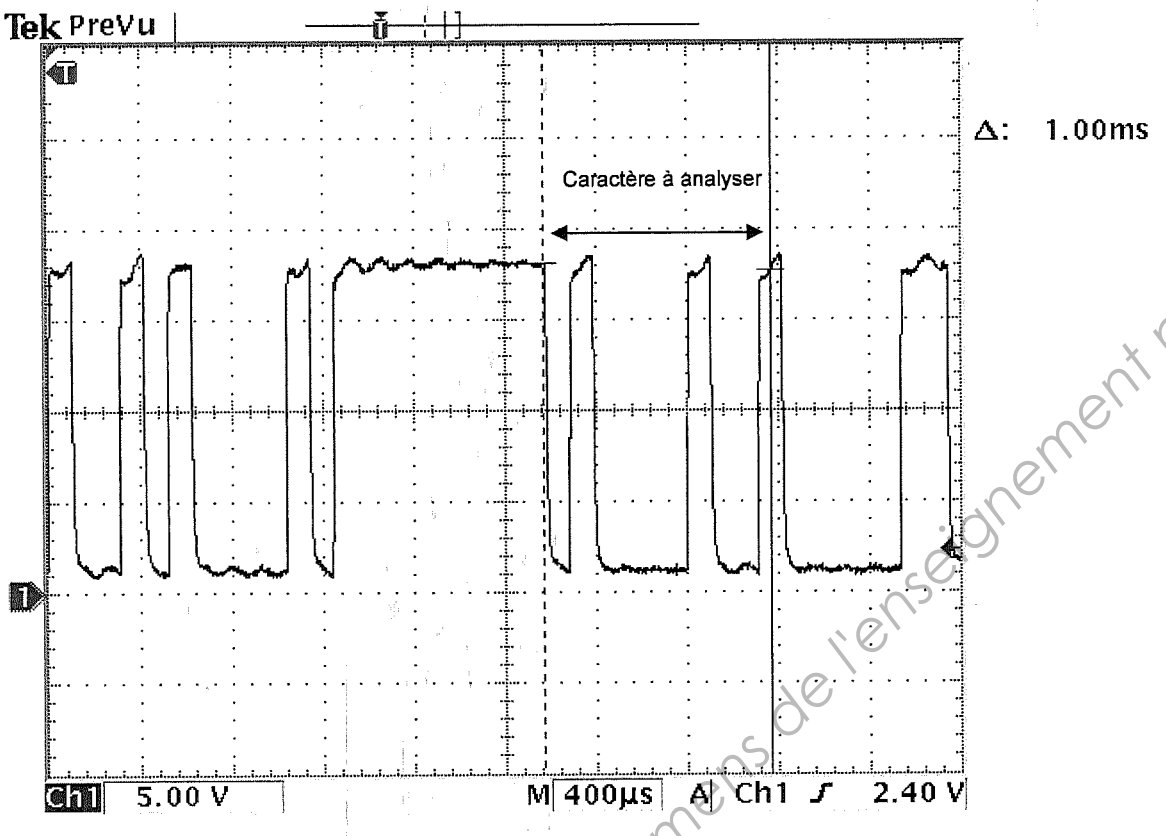
Q36.



Q37.

```
unsigned char Init_Serial() {
    unsigned char c;

    BAUD_REG = 0x.....;      /* configure timer for the correct baud rate */
    SP_CON =0b.....;   /* Set Serial IO to receive and normal mode1*/

}
```

Q40.