BEP
Métiers de l'électronique

SYSTEME D'AFFICHAGE LUMINEUX

DOCUMENTATIONS CONSTRUCTEURS

Support des épreuves EP2 – EP3

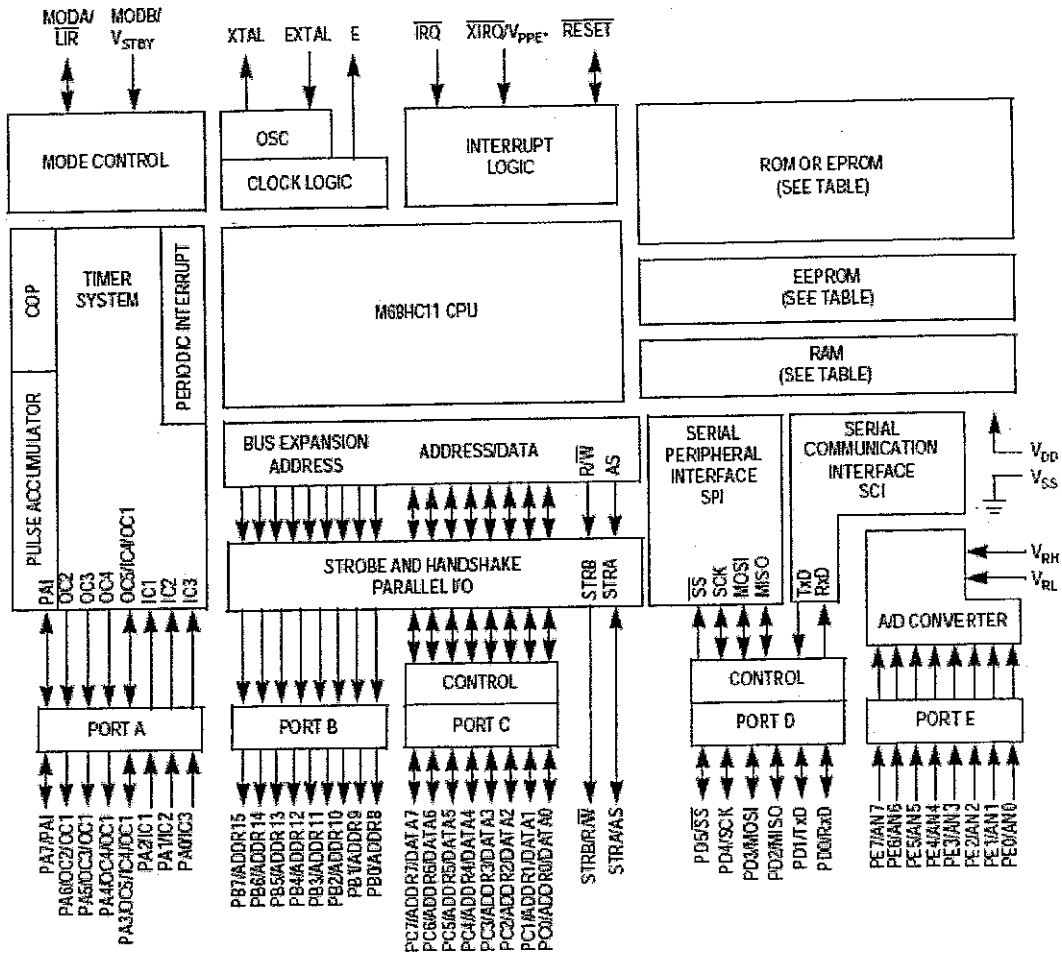
Groupement Académique Grand EST **Session 2005**

SOMMAIRE

Documentation partielle 68HC11E

Features of the E-series devices include:

- M68HC11 CPU
- Power-saving stop and wait modes
- Low-voltage devices available (3.0–5.5 Vdc)
- 0, 256, 512, or 768 bytes of on-chip RAM, data retained during standby
- 0, 12, or 20 Kbytes of on-chip ROM or EPROM
- 0, 512, or 2048 bytes of on-chip EEPROM with block protect for security
- 2048 bytes of EEPROM with selectable base address in the MC68HC811E2
- Asynchronous non-return-to-zero (NRZ) serial communications interface (SCI)
- Additional baud rates available on MC68HC(7)11E20
- Synchronous serial peripheral interface (SPI)
- 8-channel, 8-bit analog-to-digital (A/D) converter
- 16-bit timer system:
  - Three input capture (IC) channels
  - Four output compare (OC) channels
  - One additional channel, selectable as fourth IC or fifth OC
- 8-bit pulse accumulator
- Real-time interrupt circuit
- Computer operating properly (COP) watchdog system
- 38 general-purpose input/output (I/O) pins:
  - 16 bidirectional I/O pins
  - 11 input-only pins
  - 11 output-only pins



DEVICE	RAM	ROM	EPROM	EEPROM
MC68HC11E0	512	-	-	-
MC68HC11E1	512	-	-	512
MC68HC11E9	512	12 K	-	512
MC68HC711E9	512	-	12 K	512
MC68HC11E20	768	20 K	-	512
MC68HC711E20	768	-	20 K	512
MC68HC811E2	256	-	-	2048

* V_{PPE} applies only to devices with EPROM/OTPROM.

Figure 1-1. M68HC11 E-Series Block Diagram

Crystal Driver and External Clock Input (XTAL and EXTAL)

These two pins provide the interface for either a crystal or a CMOS-compatible clock to control the internal clock generator circuitry. The frequency applied to these pins is four times higher than the desired E-clock rate.

The XTAL pin must be left unterminated when an external CMOS-compatible clock input is connected to the EXTAL pin. The XTAL output is normally intended to drive only a crystal.

E-Clock Output (E)

E is the output connection for the internally generated E clock. The signal from E is used as a timing reference. The frequency of the E-clock output is one fourth that of the input frequency at the XTAL and EXTAL pins. When E-clock output is low, an internal process is taking place. When it is high, data is being accessed.

All clocks, including the E clock, are halted when the MCU is in stop mode. To reduce RFI emissions, the E-clock output of most E-series devices can be disabled while operating in single-chip modes.

The E-clock signal is always enabled on the MC68HC811E2.

MODA and MODB (MODA/$\overline{LIR}$ and MODB/V_{STBY})

During reset, MODA and MODB select one of the four operating modes:

- Single-chip mode
- Expanded mode
- Test mode
- Bootstrap mode

mory.

After the operating mode has been selected, the load instruction register ($\overline{LIR}$) pin provides an open-drain output to indicate that execution of an instruction has begun. A series of E-clock cycles occurs during execution of each instruction. The $\overline{LIR}$ signal goes low during the first E-clock cycle of each instruction (opcode fetch). This output is provided for assistance in program debugging.

The V_{STBY} pin is used to input random-access memory (RAM) standby power. When the voltage on this pin is more than one MOS threshold (about 0.7 volts) above the V_{DD} voltage, the internal RAM and part of the reset logic are powered from this signal rather than the V_{DD} input. This allows RAM contents to be retained without V_{DD} power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

MC54/74HC573A

Octal 3-State Noninverting Transparent Latch

High–Performance Silicon–Gate CMOS

The MC54/74HC573A is identical in pinout to the LS573. The devices are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

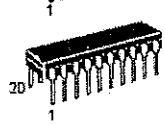
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The HC573A is identical in function to the HCT373A but has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC573A is the noninverting version of the HC563A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates

J SUFFIX
CERAMIC PACKAGE
CASE 732–03



N SUFFIX
PLASTIC PACKAGE
CASE 738–03

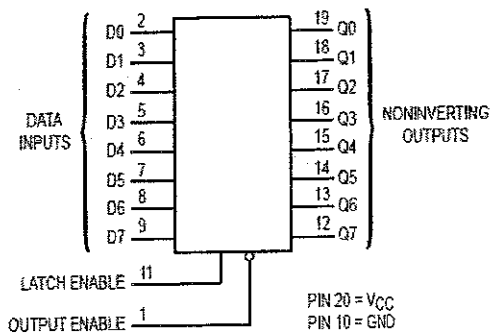
DW SUFFIX
SOIC PACKAGE
CASE 751D–04

DT SUFFIX
TSSOP PACKAGE
CASE 948E–02

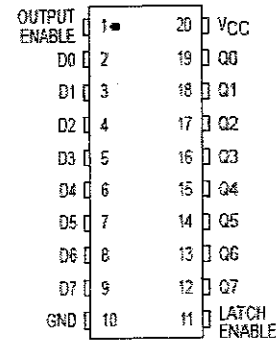
ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXADW	SOIC
MC74HCXXXADT	TSSOP

LOGIC DIAGRAM



PIN ASSIGNMENT



Design Criteria	Value	Units
Internal Gate Count*	54.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	µW
Speed Power Product	0.0075	pJ

* Equivalent to a two–input NAND gate.

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

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REV 7

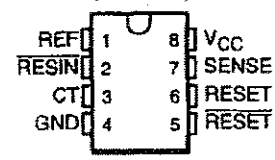
MOTOROLA

TL7702B, TL7705B, TL7702BY, TL7705BY
SUPPLY VOLTAGE SUPERVISORS

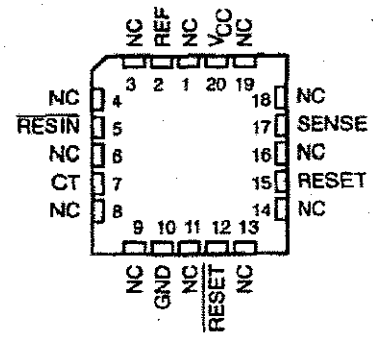
SLVS037D – SEPTEMBER 1989 – REVISED AUGUST 1995

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Output Defined From $V_{CC} \geq 1$ V**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

TL77xxBC . . . P OR D PACKAGE
TL77xxBM . . . JG PACKAGE
(TOP VIEW)



TL77xxBM . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TL7702B and TL7705B are monolithic integrated circuit voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay timer function activates a time delay after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low respectively). When an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d \approx 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 µF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

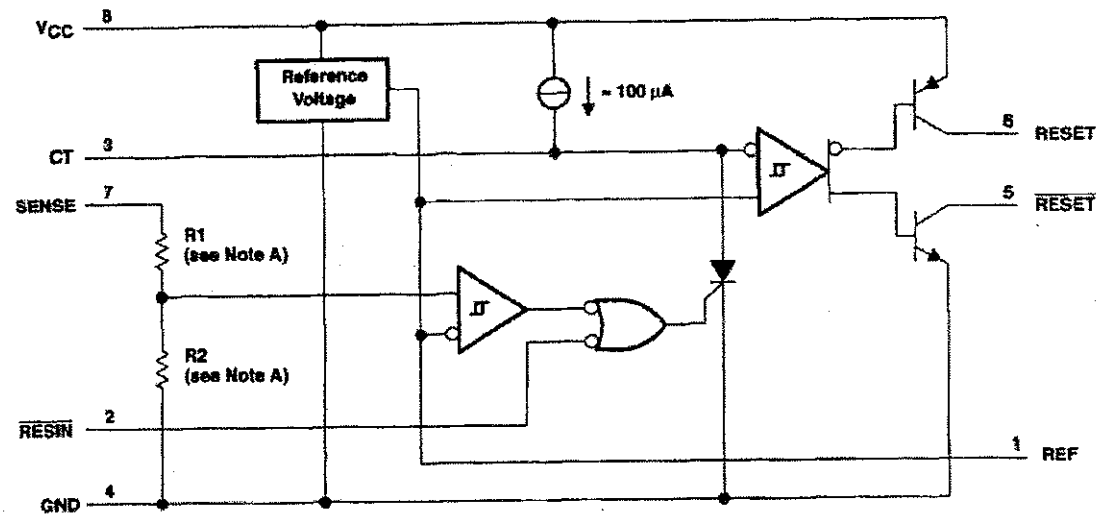
The TL7702BC and TL7705BC are characterized from 0°C to 70°C. The TL7702BI and TL7705BI are characterized for operation from −40°C to 85°C. The TL7702BQ and TL7705BQ are characterized for operation from −40°C to 125°C. The TL7702BM and TL7705BM are characterized for operation from −55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE				CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	TL7702BCD, TL7705BCD	—	—	TL7702BCP, TL7705BCP	TL7702BY TL7705BY
−40°C to 85°C	TL7702BID, TL7705BID	—	—	TL7702BIP, TL7705BIP	
−40°C to 125°C	TL7702BQD, TL7705BQD	—	—	TL7702BQP, TL7705BQP	
−55°C to 125°C	—	TL7702BMFK TL7705BMFK	TL7702BMJG TL7705BMJG	—	

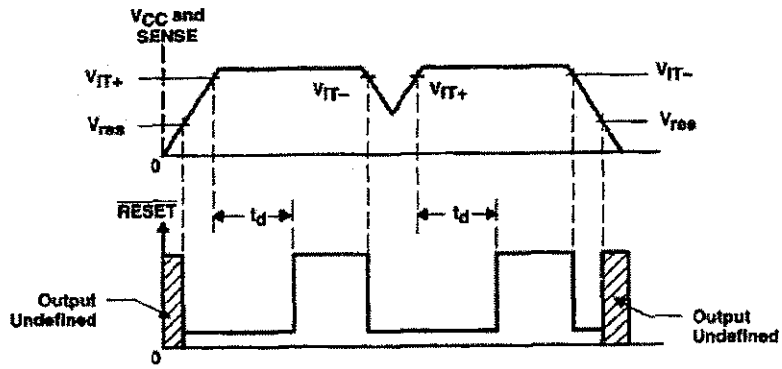
functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense comparator trip point.



NOTE A: TL7702B: R1 = 0 Ω, R2 = open
TL7705B: R1 = 23 kΩ, R2 = 10 kΩ, nominal

typical timing diagram



TL7702B, TL7705B, TL7702BY, TL7705BY SUPPLY VOLTAGE SUPERVISORS

SLVS037D – SEPTEMBER 1989 – REVISED AUGUST 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Input voltage range, V_I ($\overline{RESIN}$) ..... −0.3 V to 20 V
Input voltage range, V_I (SENSE) ..... −0.3 V to 20 V
High-level output current, I_{OH} ($\overline{RESET}$) ..... −30 mA
Low-level output current, I_{OL} ($\overline{RESET}$) ..... 30 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TL770xBC ..... 0°C to 70°C
TL770xBI ..... −40°C to 85°C
TL770xBQ ..... −40°C to 125°C
TL770xBM ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P packages ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{CC}			3.6	18	V
High-level input voltage, V_{IH}	$\overline{RESIN}$		2	18	V
Low-level input voltage, V_{IL}	$\overline{RESIN}$		0	0.8	V
Input voltage, V_I	SENSE		0	18	V
High-level output current, I_{OH}	$\overline{RESET}$			−16	mA
Low-level output current, I_{OL}	$\overline{RESET}$			16	mA
Timing capacitor, C_T				10	μF
Operating free-air temperature range, T_A		TL770xBC	0	70	°C
		TL770xBI	−40	85	
		TL770xBQ	−40	125	
		TL770xBM	−55	125	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TL77xxBC, TL77xxBI TL77xxBQ			UNIT
					MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA		V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{RESET}$		I_{OL} = 16 mA				0.4	V
V_{ref}	Reference voltage		I_{ref} = 500 µA,	T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702B	T_A = 25°C		2.505	2.53	2.555	V
		TL7705B			4.5	4.55	4.6	V
		TL7702B	T_A = Full range‡		2.48	2.53	2.58	V
		TL7705B			4.45	4.55	4.65	V
V_{hys}	Hysteresis, SENSE ($V_{IT+} - V_{IT-}$)	TL7702B	V_{CC} = 3.6 V to 18 V,			10		mV
		TL7705B	T_A = 25°C			30		mV
V_{res}§	Power-up reset voltage		I_{OL} at $\overline{RESET}$ = 2 mA, T_A = 25°C				1	V
I_I	Input current, $\overline{RESIN}$		V_I = 0.4 V to V_{CC}				–10	µA
I_I	Input current, SENSE	TL7702B	V_I = V_{ref} to 18 V			–0.1	–2	µA
I_{OH}	High-level output current, $\overline{RESET}$		V_O = 18 V,	See Figure 1			50	µA
I_{OL}	Low-level output current, RESET		V_O = 0 V,	See Figure 1			–50	µA
I_{CC}	Supply current		V_{SENSE} = 15 V,	$\overline{RESIN}$ ≥ 2 V		1.8	3	mA
			V_{CC} = 18 V	T_A = Full range‡			3.5	mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.
‡ Full range for the C-suffix device is 0°C to 70°C, full range for the I-suffix is –40°C to 85°C, and full range for the Q-suffix device is –40°C to 125°C.
§ This is the lowest voltage at which $\overline{RESET}$ becomes active.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL77xxBC, TL77xxBI TL77xxBQ			UNIT
					MIN	TYP	MAX	
t_{PLH}	Propagation delay time from low-to-high-level output	$\overline{RESIN}$	RESET	See Figures 1, 2, and 3		270	500	ns
t_{PHL}	Propagation delay time from high-to-low-level output	$\overline{RESIN}$	$\overline{RESET}$	See Figures 1, 2, and 3		270	500	ns
t_w	Effective pulse duration	$\overline{RESIN}$		See Figure 2		150		ns
		SENSE		See Figure 2		100		ns
t_r	Rise time		$\overline{RESET}$	See Figures 1 and 3			75	ns
t_f	Fall time		$\overline{RESET}$	See Figures 1 and 3		150	200	ns
t_r	Rise time		RESET	See Figures 1 and 3		75	150	ns
t_f	Fall time		RESET	See Figures 1 and 3			50	ns