3-to-8 line decoder/demultiplexer; inverting 74HC/HCT138

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT138 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).

The "138" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "138" to a 1-of-32 (5 lines to 32 lines) decoder with just four "138" ICs and one inverter.

The "138" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "138" is identical to the "238" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH} t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$ E_3 to $\overline{Y}_n$ $\overline{E}_n$ to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	 12 14	 17 19	 ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	67	67	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

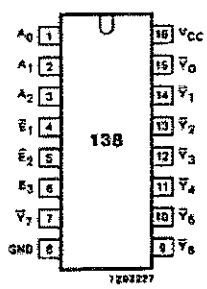


Fig.1 Pin configuration.

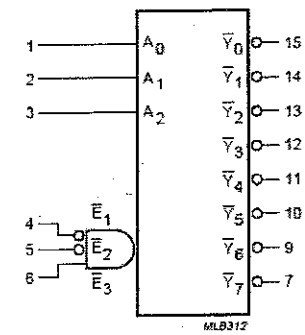


Fig.2 Logic symbol.

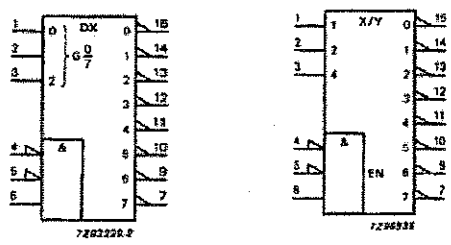


Fig.3 IEC logic symbol.

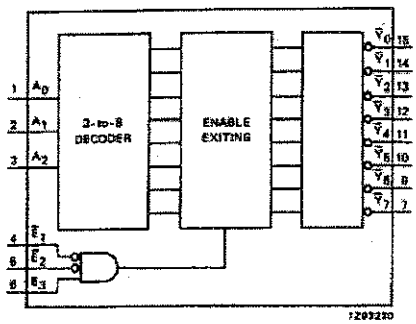


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

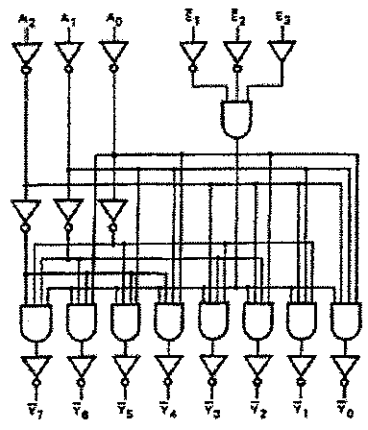


Fig.5 Logic diagram.

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

MC54/74HC574A

Octal 3-State Noninverting D Flip-Flop

High–Performance Silicon–Gate CMOS

The MC54/74HC574A is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip–flops, but when Output Enable is high, all device outputs are forced to the high–impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574A is identical in function to the HCT374A but has the flip–flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC574A is the noninverting version of the HC564.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

J SUFFIX
CERAMIC PACKAGE
CASE 732–03

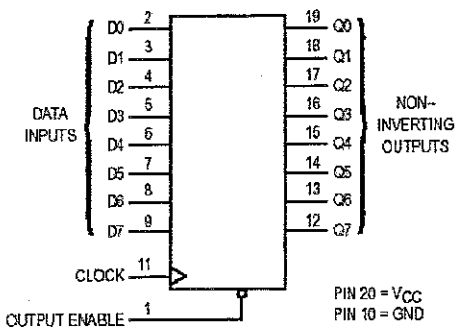
N SUFFIX
PLASTIC PACKAGE
CASE 738–03

DW SUFFIX
SOIC PACKAGE
CASE 751D–04

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXADW	SOIC

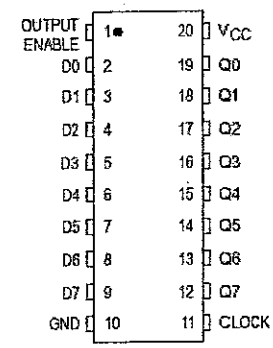
LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count*	66.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	µW
Speed Power Product	0.0075	pJ

* Equivalent to a two–input NAND gate.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
OE	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L,H,↓	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC541

Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

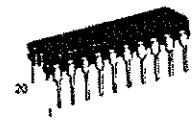
High-Performance Silicon-Gate CMOS

The MC54/74HC541 is identical in pinout to the LS541. The device inputs are compatible with standard CMOS outputs. External pullup resistors make them compatible with LSTTL outputs.

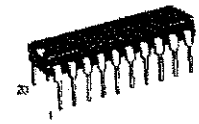
The HC541 is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC541 is similar in function to the HC540, which has inverting outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 140 FETs or 35 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

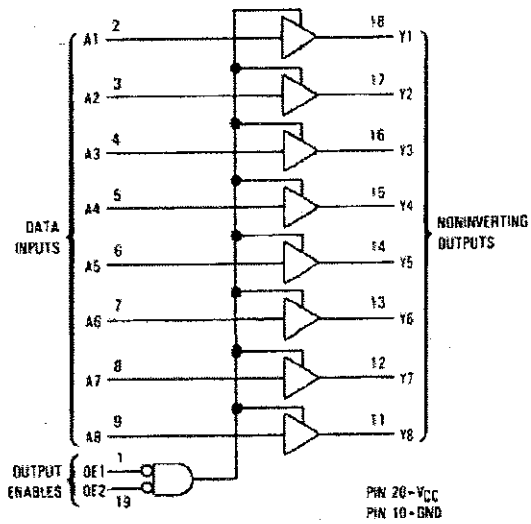
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

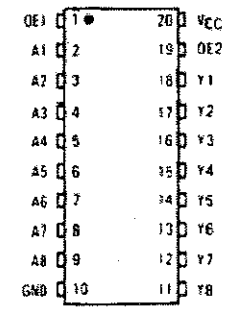
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

T_A = −55° to 125°C for all packages.
Dimensions in Chapter 6.

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

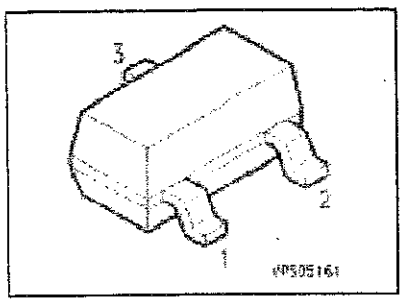
Z = high impedance
X = don't care

SIEMENS

PNP Silicon AF Transistors

BC 807
BC 808

- For general AF applications
- High collector current
- High current gain
- Low collector-emitter saturation voltage
- Complementary types: BC 817, BC 818 (NPN)



Type	Marking	Ordering Code	Pin Configuration 1	2	3	Package[1]
BC 807-16	5As	Q62702-C1735	B	E	C	SOT-23
BC 807-25	5Bs	Q62702-C1689				
BC 807-40	5Cs	Q62702-C1721				
BC 808-16	5Es	Q62702-C1736				
BC 808-25	5Fs	Q62702-C1504				
BC 808-40	5Gs	Q62702-C1692				

[1] For detailed information see chapter Package Outlines.

SIEMENS **BC 807**
BC 808

Electrical Characteristics
at T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Collector-emitter breakdown voltage I_C = 10 mA BC 807 BC 808	$V_{(BR)CE0}$	 45 25	 – –	 – –	V
Collector-base breakdown voltage I_C = 100 µA BC 807 BC 808	$V_{(BR)CB0}$	 50 30	 – –	 – –	
Emitter-base breakdown voltage, I_E = 10 µA	$V_{(BR)EB0}$	5	–	–	
Collector cutoff current V_{CB} = 25 V V_{CB} = 25 V, T_A = 150 °C	I_{CB0}	 – –	 – –	 100 50	 nA µA
Emitter cutoff current, V_{EB} = 4 V	I_{EB0}	–	–	100	nA
DC current gain[1] I_C = 100 mA; V_{CE} = 1 V BC 807-16, BC 808-16 BC 807-25, BC 808-25 BC 807-40, BC 808-40 I_C = 300 mA; V_{CE} = 1 V BC 807-16, BC 808-16 BC 807-25, BC 808-25 BC 807-40, BC 808-40	h_{FE}	 100 160 250 60 100 170	 160 250 350 – – –	 250 400 630 – – –	–
Collector-emitter saturation voltage[1] I_C = 500 mA; I_B = 50 mA	V_{CEsat}	–	–	0.7	V
Base-emitter saturation voltage[1] I_C = 500 mA; I_B = 50 mA	V_{BEsat}	–	–	2	
AC characteristics					
Transition frequency I_C = 50 mA, V_{CE} = 5 V, f = 20 MHz	f_t	–	200	–	MHz
Output capacitance V_{CB} = 10 V, f = 1 MHz	C_{obo}	–	10	–	pF
Input capacitance V_{EB} = 0.5 V, f = 1 MHz	C_{ibo}	–	60	–	

[1] Pulse test: $t \leq 300$ µs, $D \leq 2$ %.

3-to-8 line decoder/demultiplexer 74HC/HCT238

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT238 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active HIGH outputs (Y_0 to Y_7).
The "238" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be LOW unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "238" to a 1-of-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter.

The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "238" is identical to the "138" but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	A_n to Y_n		14	18	ns
	E_3 to Y_n		16	20	ns
	$\overline{E}_n$ to Y_n		17	21	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	72	76	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

3-to-8 line decoder/demultiplexer 74HC/HCT238

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y_0 to Y_7	outputs (active HIGH)
16	V_{CC}	positive supply voltage

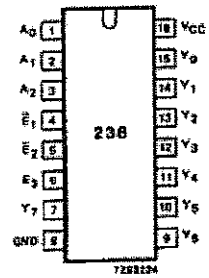


Fig.1 Pin configuration.

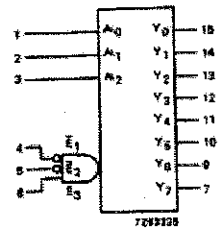
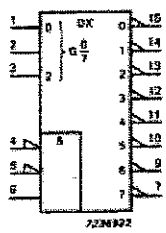
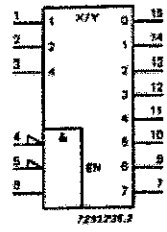


Fig.2 Logic symbol.



(a)



(b)

Fig.3 IEC logic symbol.

3-to-8 line decoder/demultiplexer 74HC/HCT238

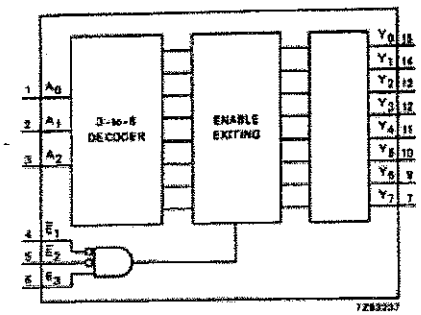


Fig.4 Functional diagram.

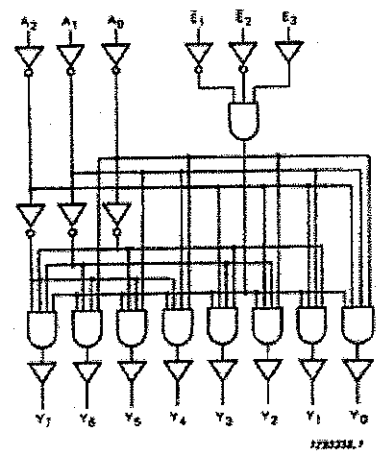


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Note

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care