L291-1/5

L291

5 BIT - D/A CONVERTER AND POSITION AMPLIFIER

The L291, a monolithic LSI circuit in a 16-lead dual in-line plastic package, is intended for use with the L290 and L292 to form a complete 3 chip DC motor positioning system for applications such as carriage/daisy-wheel position control in typewriters.

The L290/291/292 system can be directly controlled by a microprocessor.

The L291 integrates the following functions:

- 5 bit D/A converter (½ LSB max linearity error);
- error amplifier;
- position amplifier.

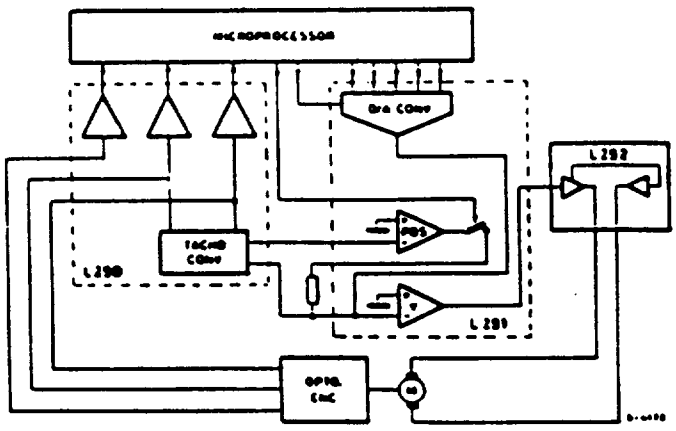
DIP-16 Plastic
(0.4)

ORDERING NUMBER: L291B

ABSOLUTE MAXIMUM RATINGS

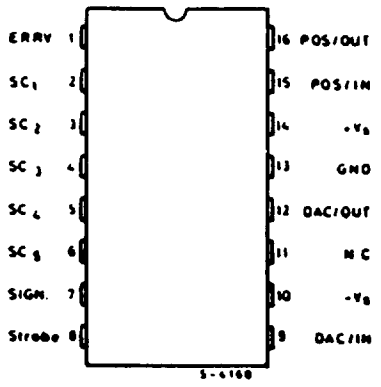
V_s	Supply voltage	± 15	V
P_{tot}	Total power dissipation T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

SYSTEM BLOCK DIAGRAM

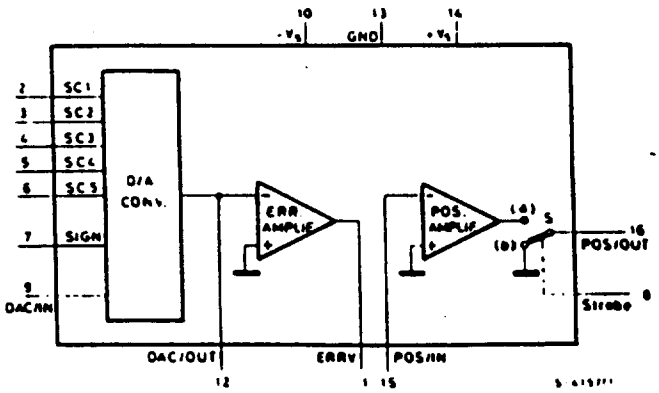


L291-2/5

CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



D/A Converter

The L291 contains a 5-bit D/A converter accepting a binary code and generating a bipolar output current, the polarity of which depends on the SIGN input. The amplitude of the output current is a multiple of a reference current I_{ref}.
The maximum output current is

$$I_{FS} = \pm \frac{31}{16} I_{ref}$$

The following table shows the value of I_o for different input codes. Note that the input bits are active low.

DIGITAL INPUT WORD						Output Current I_o
SIGN	SC5 MSB	SC4	SC3	SC2	SC1 LSB	
L	L	L	L	L	L	$-\frac{31}{16} I_{ref}$
L	H	H	H	H	L	$-\frac{1}{16} I_{ref}$
X	H	H	H	H	H	0
H	H	H	H	H	L	$+\frac{1}{16} I_{ref}$
H	L	L	L	L	L	$+\frac{31}{16} I_{ref}$

X = indifferent
L = low
H = high

This D/A converter has a maximum linearity error equal to ± 1/2 LSB (or ± 1.61% Full Scale): that guarantees its monotonicity.

Error Amplifier

In order to have a good stability, the Error Amplifier must work with a closed loop gain greater or equal than 20 dB.

Position Amplifier

It is inserted by means of the strobe signal, TTL and microprocessor compatible. Its output is connected to pin 16 when V_{strobe} = Low; pin 16 is grounded for V_{strobe} = High.

SYSTEM DESCRIPTION: refer to the L292 data sheet.

National Semiconductor

Industrial Blocks

LM556/LM556C Dual Timer

General Description

The LM556 Dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

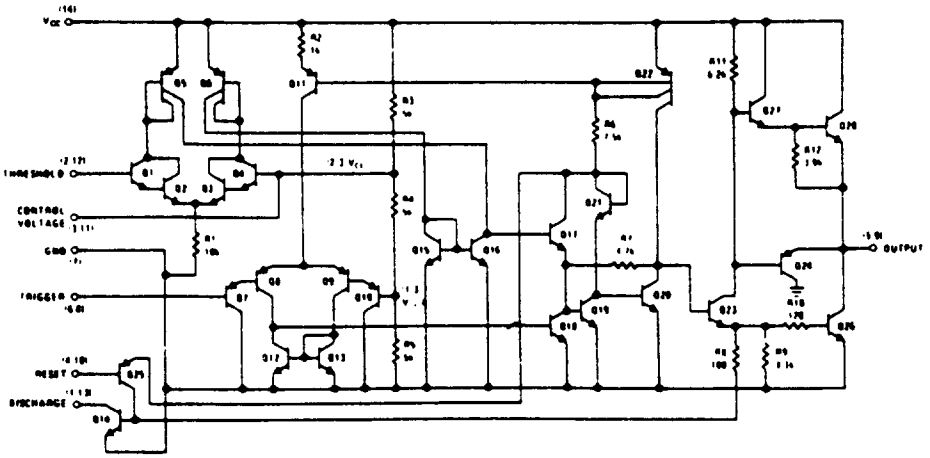
Features

- Direct replacement for SE556/NE556
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

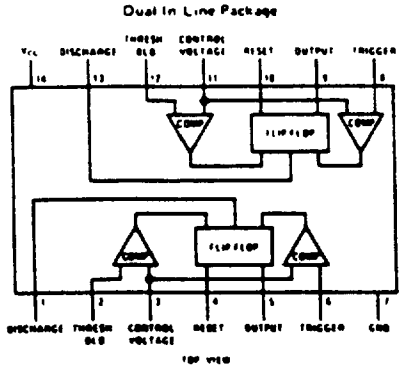
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagram

Dual In Line Package



Order Number LM556CN
See NS Package N14A

Order Number LM556J or LM556CJ
See NS Package J14A

Absolute Maximum Ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM556C	0°C to +70°C
LM556	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LM556			LM556C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
(Each Timer Section)	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	11		10	14	mA
Timing Error, Monostable								
Initial Accuracy			0.5			0.75		%
Drift With Temperature	R_A, R_B = 1k to 100k, C = 0.1μF (Note 3)		30			50		ppm/°C
Accuracy Over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift With Temperature			90			150		ppm/°C
Accuracy Over Temperature			2.5			3.0		%
Drift With Supply			0.15			0.30		%/V
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2	4.5	5	5.5	V
	V_{CC} = 5V	1.45	1.67	1.9	1.25	1.67	2.0	V
Trigger Current			0.1	0.5		0.2	1.0	μA
Reset Voltage	(Note 4)	0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.6	mA
Threshold Current	(Note 5)		0.03	0.1		0.03	0.1	μA
Control Voltage Level And	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
Threshold Voltage	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 1, 13 Leakage Output High			1	100		1	100	nA
Pin 1, 13 Set	(Note 6)							
Output Low	V_{CC} = 15V, I_{SINK} = 15 mA		150	240		180	300	mV
Output Low	V_{CC} = 4.5V, I_{SINK} = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.25		2	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Matching Characteristics	(Note 7)							
Initial Timing Accuracy			0.05	0.2		0.1	2.0	%
Timing Drift With Temperature			±10			±10		ppm/°C
Drift With Supply Voltage			0.1	0.2		0.2	0.6	%/V

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: As reset voltage lowers, timing is inhibited and then the output goes low.

Note 5: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 6: No protection against excessive pin 1, 13 current is necessary providing the package dissipation rating will not be exceeded.

Note 7: Matching characteristics refer to the difference between performance characteristics of each timer section.

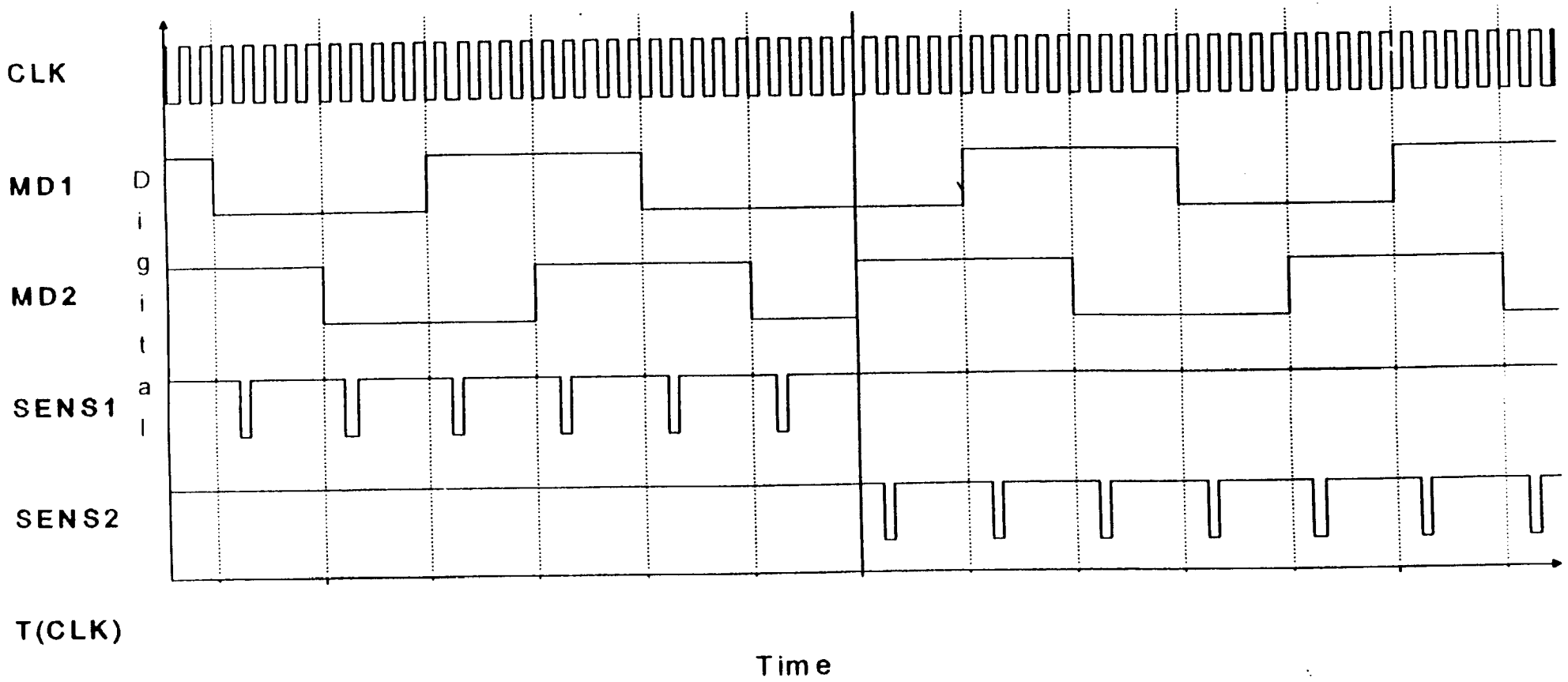
NOMENCLATURE DES COMPOSANTS

Carte PC 340 GH

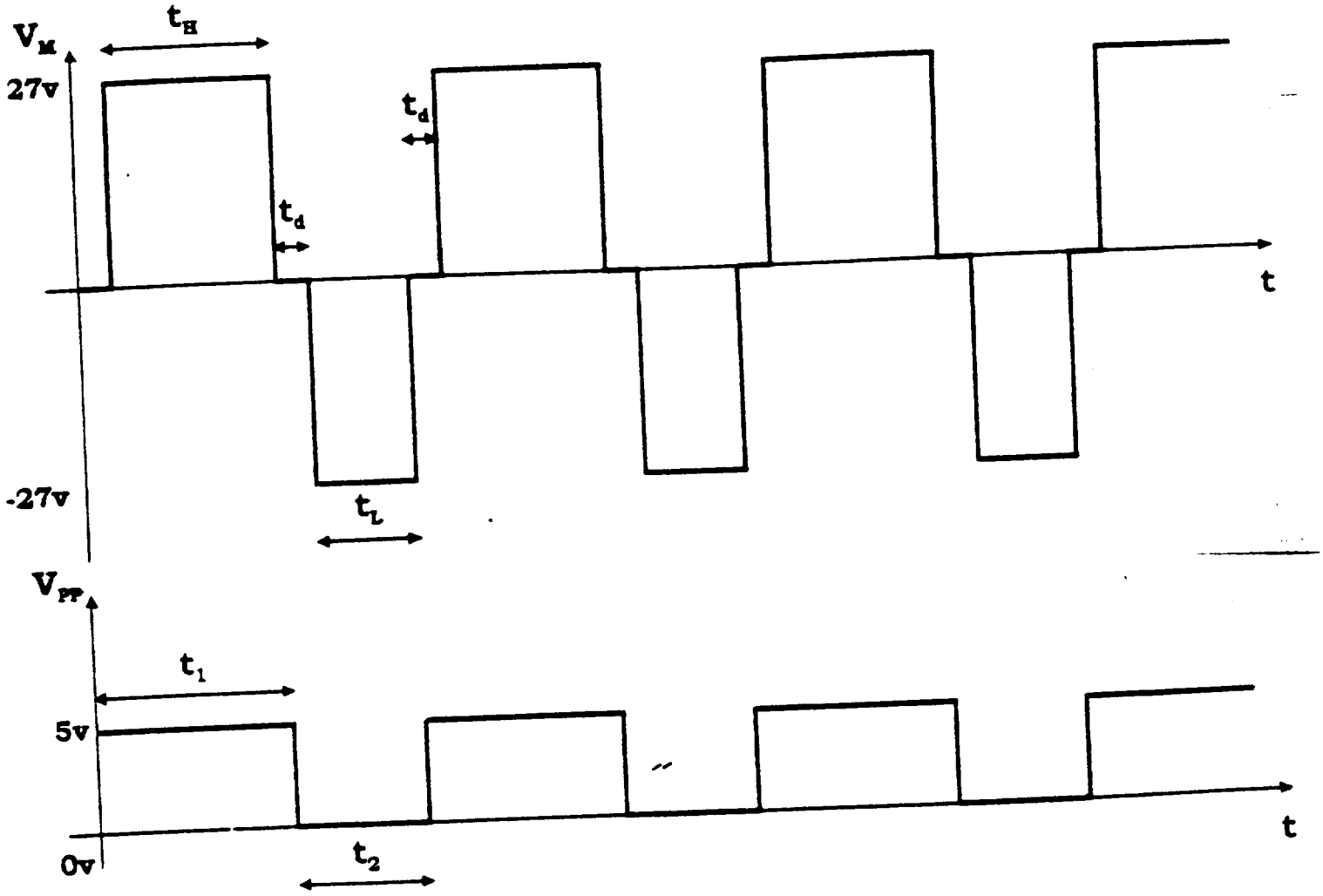
R1	1KΩ	R46	10KΩ	C48	0.1uF	D8	1N4148
R2	22KΩ	R47	10KΩ	C49	10nF	D9	1N4148
R3		R48	4.7KΩ	C50	10nF	D10	1N4148
R4	1KΩ	R49	4.7KΩ	C51	10nF	D11	1N5624
R5	1KΩ	R50	1.2KΩ			D12	1N5624
R6	56KΩ	R51	1.2KΩ	IC1	LS123	D13	1N5624
R7	10KΩ	R52	100Ω	IC2	7556	D14	1N5624
R8	10KΩ	R53	100Ω	IC3	LS86	D15	HSCH1001
R9	560KΩ	R54	6.8KΩ	IC4	LS154	D16	HSCH1001
R10	22KΩ	R55	33Ω	IC5	LS74		
R11	22KΩ	R56	100Ω	IC6	LS74	TR1	2N2905A
R12	15KΩ	R57	390Ω	IC7	LS74	TR2	*
R13	22KΩ	R58	390Ω	IC8	DAC800	TR3	*
R14	15KΩ	R59	470Ω	IC9	UA741	TR4	2N2905A
R15	22KΩ	R60	470Ω	IC10	UA741	TR5	*
R16	56KΩ			IC11	78HC05	TR6	*
R17	56KΩ	RV1	20KΩ	IC12	LS14	TR7	ME4102
R18	56KΩ			IC13	LS20	TR8	ME4102
R19	10KΩ	C2	2.2nF	IC14	LS00	TR9	BCX38A
R20	470Ω	C5	10nF	IC15	LS193		
R21	470KΩ	C9	2.2uF	IC16	LS193	OC1	4N26
R22	150KΩ	C10	2.2uF	IC17	LS193	OC2	4N26
R23	2.2KΩ	C11	100pF	IC18	UA741	OC3	HCPL2630
R24	39KΩ	C12	100pF	IC19	LM311		
R25	6.8KΩ	C15	0.1uF	IC20	LS138	L1	1uH
R26	220Ω	C16	0.1uF	IC21	4118/8128		
R27	100Ω	C19	0.1uF	IC22	2516/2532	X1	1MHz
R28	470Ω	C20	0.1uF	IC23	LS10		
R29	470Ω	C21	1nF	IC24	LS14		
R30	220Ω	C23	4.7nF	IC25	L291		
R31	1.2KΩ	C29	2.2uF	IC26	7812		
R32	1.8KΩ	C30	2.2uF	IC27	7912		
R33	1.8KΩ	C31	2.2uF	IC28	LS04		
R34	220Ω	C32	2.2uF	IC29	6502		
R35	1.2KΩ	C33	220pF	IC30	6520		
R36	1.8KΩ	C34	2.2uF	IC31	6520		
R37	1.8KΩ	C39	0.1uF	IC32	6520		
R38	2.7KΩ	C40	0.1uF				
R39	1MΩ	C41	0.1uF	D1	1N4148		
R40	68KΩ	C42	0.1uF	D2	HSCH1001		
R41	220KΩ	C43	0.1uF	D3	1N5624		
R42	3.3KΩ	C44	4.7uF	D4	HSCH1001		
R43	68KΩ	C45	1nF	D5	1N5624		
R44	3.3KΩ	C46	470p	D6	BZY88C		
R45	3.3KΩ	C47	470p	D7	BZY88C		

Détection synchronisée du sens de déplacement suivant l'axe Z

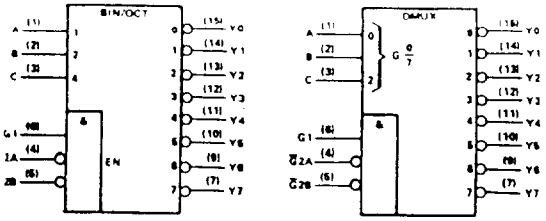
Simulation VIEW*logic*



CHRONOGRAMMES RELATIFS A V_M ET V_{PP}



138 — Décodeur-démultiplexeur 3 vers 8
3-line-to-8-line decoder/demultiplexer

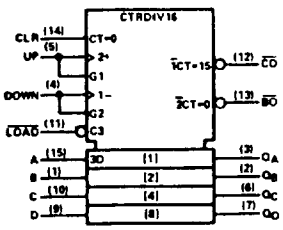


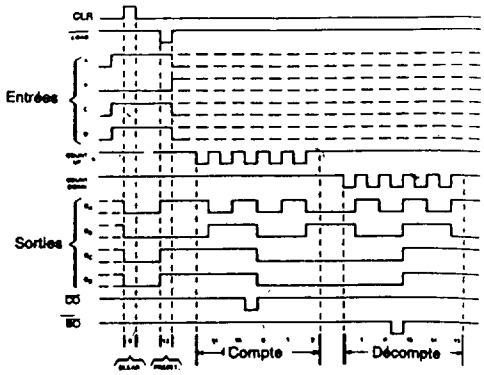
Entrées					Sorties							
Valid		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

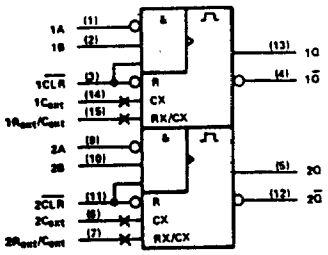
Boîtier DIL 16 - V_{CC} 16 - *GND* 8

193 — Compteur-décompteur binaire synchrone
4 bits avec 2 horloges et RAZ
Synchronous 4-bit binary UP/DOWN counter with dual clock and clear

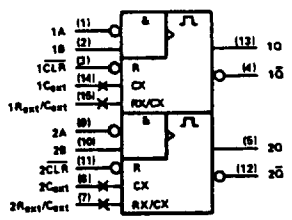




Deux monostables redéclenchables avec RAZ
Dual retriggerable monostable multivibrator with clear



		Entrées			Sorties	
123	423	CLR	A	B	Q	Q̄
		L	X	X	L	H
		X	H	X	L	H
		X	X	L	L	H
		H	L	↓	⊓	⊔
		H	↓	H	⊓	⊔
		↑	L	H	⊓	⊔



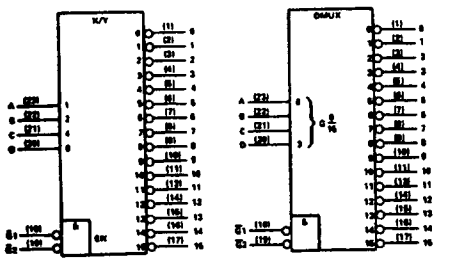
Boîtier DIL 16 - V_{CC} 16 - *GND* 7

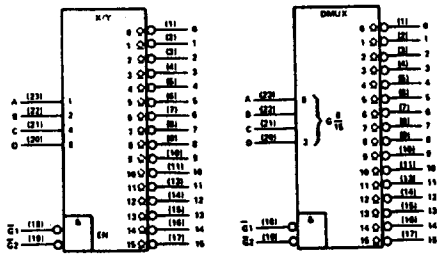
154

Décodeur-démultiplexeur 4 vers 16
4-line-to-16-line decoder/demultiplexer

159

159 — collecteur ouvert





Entrées						Sorties													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Boîtier DIL 24
V_{CC} 24 - *GND* 12

15